Agilent N5393B PCI Express Automated Test Application

Compliance Testing Methods of Implementation

Agilent Technologies

Notices

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PCI Express Automated Testing—At A Glance

The Agilent N5393B PCI Express Automated Test Application helps you verify PCI Express device under test (DUT) compliance to specifications with the Agilent 54855A, 80000B, or 90000A Infiniium digital storage oscilloscope. The PCI Express Automated Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Provides detailed information for each test that has been run and lets you specify the thresholds at which marginal or critical warnings appear.
- Creates a printable HTML report of the tests that have been run.

NOTE The tests performed by the PCI Express Automated Test Application are intended to provide a quick check of the electrical health of the DUT. This testing is not a replacement for an exhaustive test validation plan.

Required Equipment and Software

In order to run the PCI Express automated tests, you need the following equipment and software:

- N5393B PCI Express Automated Test Application software.
- Version 05.60 or greater of Infiniium software (54855A and 80000B series Infiniium Digital Storage Oscilloscope) OR
- Version 01.40.0004 of the baseline software (90000A series Infiniium Digital Storage Oscilloscope).
- 54855A Infiniium Digital Storage Oscilloscope (minimum requirement for PCI Express 1.0a, PCI Express 1.1 and Express Card 1.0 only) OR
- 80000B series Infiniium Digital Storage Oscilloscope OR
- 90000A series Infiniium Digital Storage Oscilloscope
- E2688A Serial Data Analysis and Clock Recovery software.
- Probes and/or test fixtures. For more information on the specific probes and test fixtures required, refer to the chapters that describe tests.
- N5380A Hi-BW differential SMA probe heads.
- Keyboard, qty = 1, (provided with the Agilent 54855A, 80000B, or 90000A oscilloscopes).
- Mouse, qty = 1, (provided with the Agilent 54855A, 80000B, or 90000A oscilloscopes).

- Precision 3.5 mm BNC to SMA male adapter, Agilent p/n 54855-67604, qty = 2 (provided with the Agilent 54855A, 80000B, or 90000A oscilloscopes).
- 50-ohm Coax Cable with SMA Male Connectors – 24-inch or less RG-316/U or similar, qty = 2, matched length.

In This Book

This manual describes the tests that are performed by the PCI Express Automated Test Application in more detail; it contains information from (and refers to) the Base Specification, Card Electromechanical Specification, and ExpressCard Standard, and it describes how the tests are performed.

This manual is divided to several sections:

- Part I, "Introduction" covers the software and license installation and test preparation guide.
- Part II, "PCI Express Version 1.0a" covers the tests and Method of Implementation of PCI Express version 1.0a.
- Part III, "PCI Express Version 1.1" covers the tests and Method of Implementation of PCI Express version 1.1.
- Part IV, "2.5 GT/s PCI Express Version 2.0" covers the tests and Method of Implementation of 2.5 GT/s PCI Express version 2.0.
- Part V, "5.0 GT/s PCI Express Version 2.0" covers the tests and Method of Implementation of 5.0 GT/s PCI Express version 2.0.
- Part VI, "ExpressCard 1.0" covers the tests and Method of Implementation of ExpressCard version 1.0.
- Part VII, "Appendices" covers oscilloscope calibration, channel de-skew calibration and probe information.

The chapters in this book are:

- Chapter 1, "Installing the PCI Express Automated Test Application" shows how to install and license the automated test application software (if it was purchased separately).
- Chapter 2, "Preparing to Take Measurements" shows how to start the PCI Express Automated Test Application and gives a brief overview of how it is used.
- Chapter 3, "Transmitter (Tx) Tests, PCI-E 1.0a, Full Power" contains more information on the PCI Express version 1.0a transmitter tests.
- Chapter 4, "Receiver (Rx) Tests, PCI-E 1.0a" contains more information on the PCI Express version 1.0a receiver tests.
- Chapter 5, "Add-In Card (Tx) Tests, PCI-E 1.0a" contains more information on the PCI Express version 1.0a add-in card tests.

- Chapter 6, “System Board (Tx) Tests, PCI-E 1.0a” contains more information on the PCI Express version 1.0a system board tests.
- Chapter 7, “Reference Clock Tests, PCI-E 1.1” contains more information on the PCI Express version 1.1 reference clock tests.
- Chapter 8, “Transmitter (Tx) Tests, PCI-E 1.1, Full Power” contains more information on the PCI Express version 1.1 transmitter tests.
- Chapter 10, “Receiver (Rx) Tests, PCI-E 1.1” contains more information on the PCI Express version 1.1 receiver tests.
- Chapter 11, “Add-In Card (Tx) Tests, PCI-E 1.1” contains more information on the PCI Express version 1.1 add-in card tests.
- Chapter 12, “System Board (Tx) Tests, PCI-E 1.1” contains more information on the PCI Express version 1.1 system board tests.
- Chapter 12, “Transmitter (Tx) Tests, 2.5 GT/s, PCI-E 2.0, Full Power” contains more information on the PCI Express version 2.0, 2.5 GT/s transmitter tests.
- Chapter 13, “Receiver (Rx) Tests, 2.5 GT/s, PCI-E 2.0” contains more information on the PCI Express version 2.0, 2.5 GT/s receiver tests.
- Chapter 14, “Add-In Card (Tx) Tests, 2.5 GT/s, PCI-E 2.0” contains more information on the PCI Express version 2.0, 2.5 GT/s add-in card tests.
- Chapter 15, “System Board (Tx) Tests, 2.5 GT/s, PCI-E 2.0” contains more information on the PCI Express version 2.0, 2.5 GT/s system board tests.
- Chapter 16, “Transmitter (Tx) Tests, 5.0 GT/s, PCI-E 2.0” contains more information on the PCI Express version 2.0, 5.0 GT/s transmitter tests.
- Chapter 17, “Receiver (Rx) Tests, 5.0 GT/s, PCI-E 2.0” contains more information on the PCI Express version 2.0, 5.0 GT/s receiver tests.
- Chapter 18, “Add-In Card (Tx) Tests, 5.0 GT/s, PCI-E 2.0” contains more information on the PCI Express version 2.0, 5.0 GT/s add-in card tests.
- Chapter 19, “System Board (Tx) Tests, 5.0 GT/s, PCI-E 2.0” contains more information on the PCI Express version 2.0, 5.0 GT/s system board tests.
- Chapter 20, “ExpressCard Tests” contains more information on the ExpressCard version 1.0 module and host tests.
- Appendix A, “Calibrating the Digital Storage Oscilloscope” describes how to calibrate the oscilloscope in preparation for running the PCI Express automated tests.
- Appendix C, “INF_SMA_Deskew.set Setup File Details” describes a setup used when performing channel de-skew calibration.
- Appendix B, “InfiniiMax Probing Options” describes the probe amplifier and probe head recommendations for PCI Express testing.

See Also

- The PCI Express Automated Test Application's online help, which describes:
  - Starting the PCI Express Automated Test Application
  - Creating or opening a test project.
  - Setting up the PCI Express test environment.
  - Selecting tests.
  - Configuring selected tests.
  - Connecting the oscilloscope to the DUT.
  - Running tests.
  - Viewing test results.
  - Viewing/printing the HTML test report.
  - Saving test projects.

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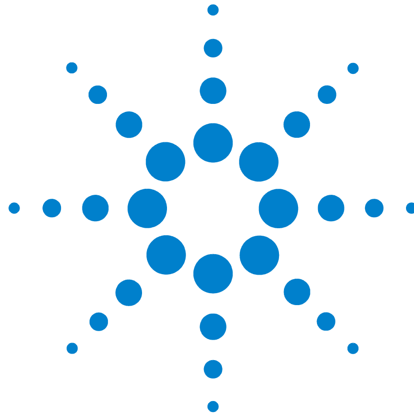

Part I
Introduction

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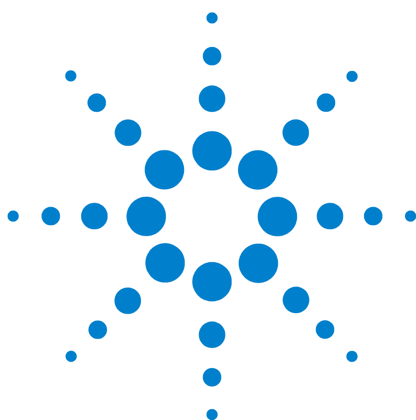

1
Installing the PCI Express Automated Test Application

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If you purchased the N5393B PCI Express Automated Test Application separately, you need to install the software and license key.

Installing the Software

1 Make sure you have version 1.40.0004 or greater of the Infiniium software (90000A series Infiniium Digital Storage Oscilloscope) OR version 5.60 or greater of the Infiniium software (80000B series Infiniium Digital Storage Oscilloscope) by choosing **Help>About Infiniium...** from the main menu.

2 To obtain the PCI Express Automated Test Application, go to Agilent website: http://www.agilent.com/find/N5393B

3 The link for PCI Express Automated Test Application will appear. Double-click on it and follow the instructions to download and install the application software.

   Be sure to accept the installation of the .NET Framework software; it is required in order to run the PCI Express Automated Test Application.

Installing the License Key

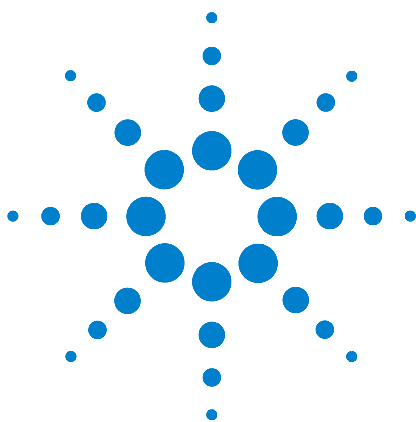
1 Request a license code from Agilent by following the instructions on the Entitlement Certificate.

   You will need the oscillocope's "Option ID Number", which you can find in the **Help>About Infiniium...** dialog.

2 After you receive your license code from Agilent, choose **Utilities>Install Option License...**.

3 In the Install Option License dialog, enter your license code and click **Install License**.

4. Click **OK** in the dialog that tells you to restart the Infiniium oscilloscope application software to complete the license installation.
5. Click **Close** to close the Install Option License dialog.
6. Choose **File>Exit**.
7. Restart the Infiniium oscilloscope application software to complete the license installation.



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Before running the PCI Express automated tests, you should calibrate the oscilloscope. After the oscilloscope has been calibrated, you are ready to start the PCI Express Automated Test Application and perform measurements.

Calibrating the Oscilloscope

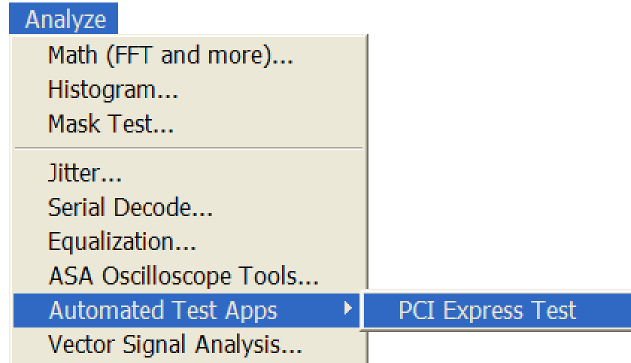
If you haven't already calibrated the oscilloscope, see Appendix A, "Calibrating the Digital Storage Oscilloscope".

NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

NOTE If you switch cables between channels or other oscilloscopes, it is necessary to perform cable and probe calibration and channel de-skew calibration again. Agilent recommends that, once calibration is performed, you label the cables with the channel they were calibrated for.

Starting the PCI Express Automated Test Application

1 From the Infiniium oscilloscope's main menu, choose Analyze>Automated Test Apps>PCI Express.



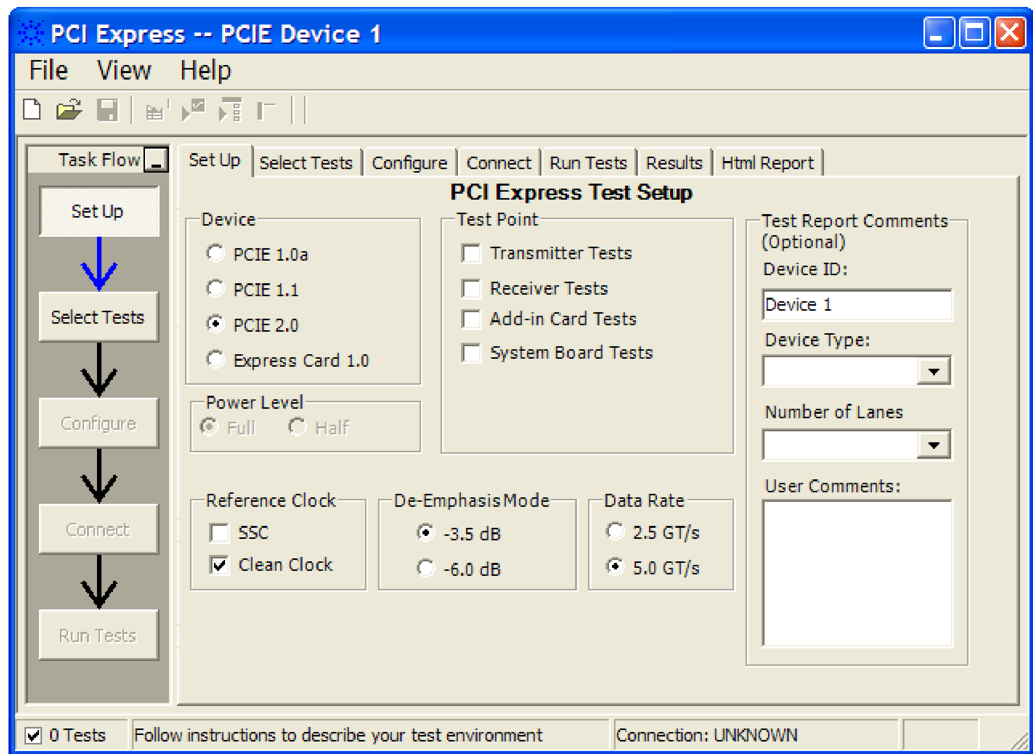


Figure 1 The PCI Express Automated Test Application

NOTE

If PCI Express does not appear in the Automated Test Apps menu, the PCI Express Automated Test Application has not been installed (see Chapter 1, "Installing the PCI Express Automated Test Application").

Figure 1 shows the PCI Express Automated Test Application main window. The task flow pane, and the tabs in the main pane, show the steps you take in running the automated tests:

Set Up	Lets you identify and setup the test environment, including information about the device under test.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you configure the test parameters (like memory depth). This information appears in the HTML report.
Connect	Shows you how to connect the oscilloscope to the device under test for the tests to be run.
Run Tests	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

Online Help Topics

For information on using the PCI Express Automated Test Application, see its online help (which you can access by choosing Help>Contents... from the application's main menu).

The PCI Express Automated Test Application's online help describes:

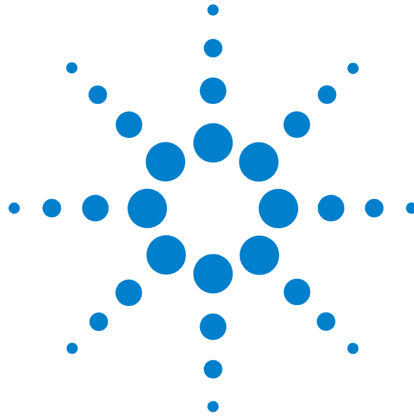
- Starting the PCI Express Automated Test Application.
  - To view or minimize the task flow pane.
  - To view or hide the toolbar.
- Creating or opening a test project.
- Setting up the test environment.
- Selecting tests.
- Configuring selected tests.
- Connecting the oscilloscope to the Device Under Test (DUT).

- Running tests.
- Viewing test results.
  - To show reference images and flash mask hits.
  - To change margin thresholds.
- Viewing/printing the HTML test report.
- Saving test projects.

Clock Recovery and Analysis (Applicable to PCI Express 1.0a Only)

As described in Section 4.3.3.1 of the Base Specification, the following methodology is used to define the data set for all PCI Express eye and jitter measurements.

- The clock recovery window is 3500 consecutive Unit Intervals and the Mean of the UIs is used as the reference clock. The first 3500 UIs in the acquisition are used.
- An analysis window is established to be 250 bits centered in the 3500 UI clock recovery window. The mask is placed based on the median of the 250 bit analysis window.
- If there are enough data points in the record, the clock recovery window is advanced by 100 UI, a new mean UI is computed, and analysis is repeated over the middle 250 UI. This process is repeated until the advancing clock recovery window passes the end of the data record.



Part II
PCI Express Version 1.0a

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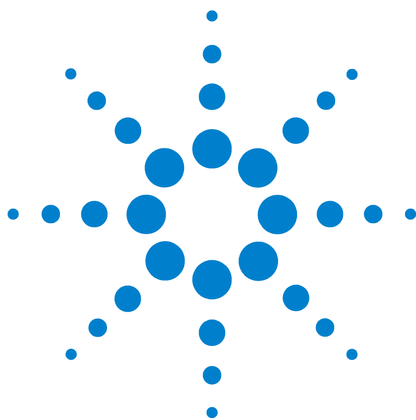

3
Transmitter (Tx) Tests, PCI-E 1.0a, Full Power

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This section provides the Methods of Implementation (MOIs) for Transmitter tests using an Agilent 54855A, 80000B, or 90000A series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

Probing the Link for Tx Compliance

Transmitter tests are done by connecting the device under test to a test fixture and probing the SMA connectors on the test fixture. To probe the transmitter link, you can:

- Use two 50-ohm coax cables with SMA male connectors, two precision 3.5 mm BNC to SMA male adapters (54855-67604, included with the 54855A oscilloscope), and the Ch1 and Ch3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.
- Use two differential probe heads with two 1134A probe amplifiers (with the negative lead grounded for single-ended measurements) and the Ch1 and Ch3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.
- Use one differential probe head with the 1134A probe amplifier and the Ch2 input of an oscilloscope that has 20 GS/s sample rate available on that channel.

When the link is broken and terminated into a 50 ohm load (by the test load), the Compliance Pattern defined in section 4.2.8 (Base Specification) will be transmitted.

Table 1 Probing Options for Transmitter Testing

	Probing Configurations			**Captured Waveforms**		**System Specifications**	
						54855A	
	Probing Method	**Break Serial Link**	**Channels Used**	**Differential Mode**	**Common Mode**	**System Band Width**	**Rise* Time (20-80)**
DUT Connection	Single-Ended SMA (2 x 50-Ohm SMA Cables)	Y	2	Pseudo	Yes	6 GHz	70 ps
	Single-Ended (2 x 1134A w/ Differential Probe Heads)	Y/N	2	Pseudo	Yes	6 GHz	70 ps
	Differential (1 x 1134A w/ Differential Probe Head)	Y/N	1	True	No	6 GHz	70 ps

*Typical

Single-Ended SMA Probing (Ch1) and (Ch3)

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Ch1-Ch3. The Common mode measurements are also available in this configuration from the common mode waveform (Ch1+Ch3)/2.

This probing technique requires breaking the link and terminating into the 50 ohm/side termination into the oscilloscope. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Channel-to-Channel deskew is required using this technique because two channels are used.

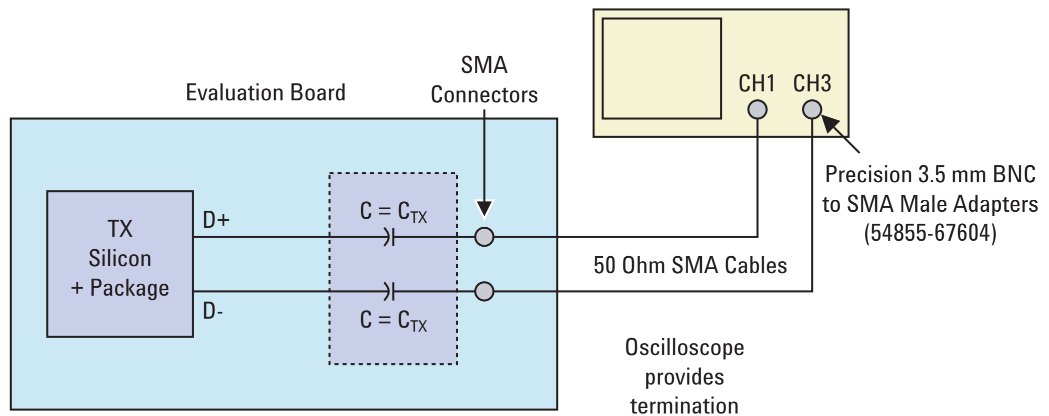


Figure 2 Single-Ended SMA Probing

Single-Ended Probing (Ch1) and (Ch3)

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Ch1-Ch3. The Common mode measurements are also available in this configuration from the common mode waveform (Ch1+Ch3)/2.

Make sure to probe equal distances from the transmitter, as close as possible to the transmitter.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Channel-to-Channel deskew is required using this technique because two channels are used.

For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 392.

Place single-ended grounds as close to the signal line’s reference ground as possible.

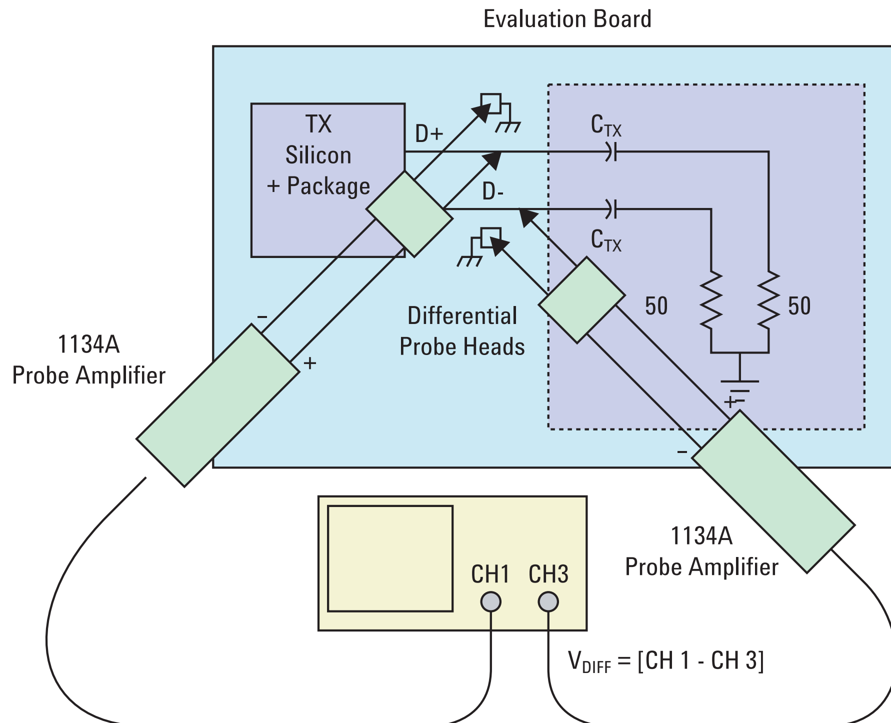


Figure 3 Single-Ended Probing

Differential Probing (Ch2)

The differential signal is measured directly by the differential probe head.

Make sure to probe equal distances from the transmitter, as close as possible to the transmitter.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Only one channel of the oscilloscope is used.

For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, "InfiniiMax Probing Options," starting on page 392.

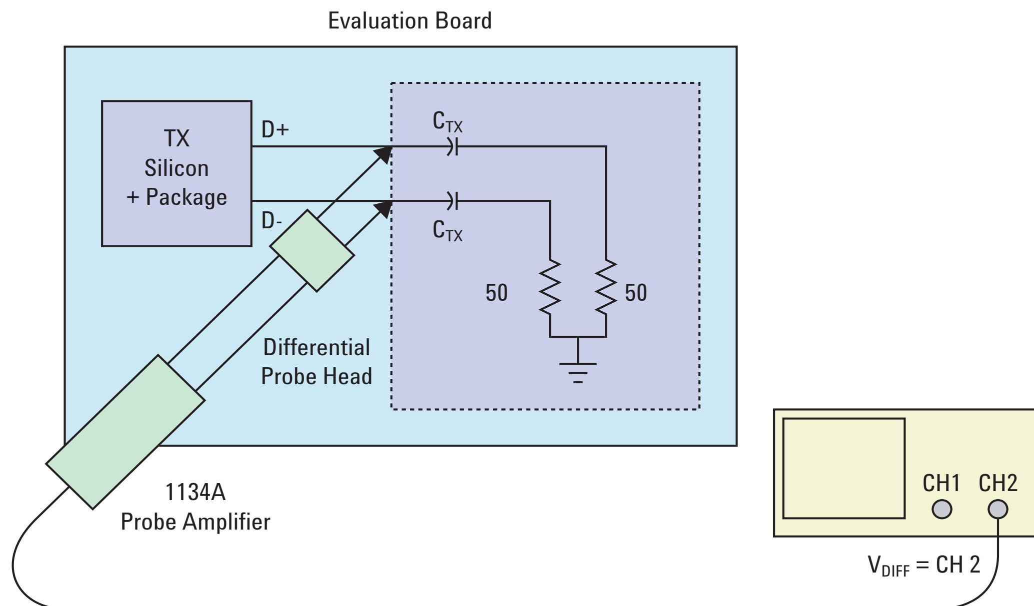


Figure 4 Differential Probing

Tx Compliance Test Load

The compliance test load for driver compliance is shown in Figure 4-25 (Base Specification)

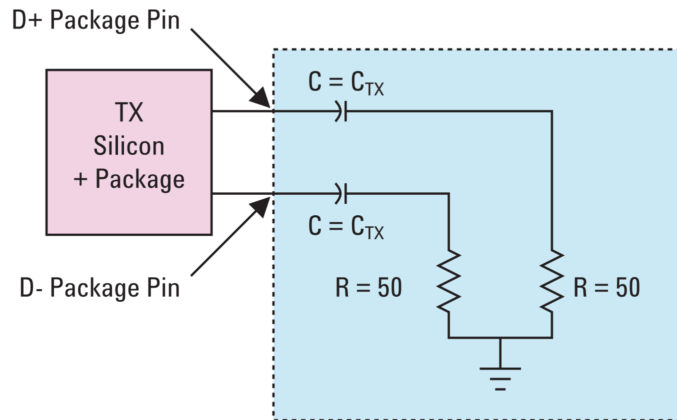


Figure 5 Driver Compliance Test Load.

Running Signal Quality Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 22. Then, when selecting tests, navigate to "Signal Quality" in the "Transmitter (Tx) Tests" group.

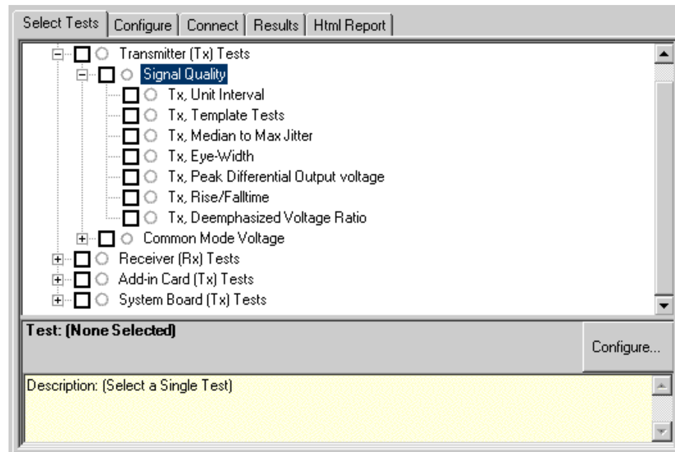


Figure 6 Selecting Transmitter (Tx) Signal Quality Tests

Tx, Unit Interval

Table 2 UI from Table 4-5 of the Base Specification.

Symbol	Parameter	Min	Nom	Max
UI	Unit Interval	399.88 ps	400ps	400.12 ps

Test Definition Notes from the Specification

- UI (Unit Interval) is specified to be +/-300 ppm.
- UI does not account for SSC dictated variations.
- UI is defined in Table 4-5 (Base Specification).
- UI Characteristics are Maximum UI =400.12 ps and Minimum UI = 399.88ps.

Test Procedure

Follow the procedure in “Running Signal Quality Tests" on page 34, and select “Unit Interval”.

PASS Condition

399.88ps < UI < 400.12ps

Measurement Algorithm

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window.

TX UI(p) = Mean(UI(n))

Where:

n is the index of UI in the current 3500 UI clock recovery window.

p indicates the pth 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI, as described below.

NOTE The TX UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another TX UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case TX UI is reported.

Test References

Table 3 Unit Interval Test References

Test Name	Reference	PCI-SIG Assertions
Unit Interval	PCI Express Base Specification, Rev 1.0a, Table 4-5	PHY.3.3#2

Tx, Template Tests

See Section 4.3.3.1 of the Base Specification for additional notes and test definitions.

Test Definition Notes from the Specification

- The TX eye diagram in Figure 4-24 (Base Specification) is specified using the passive compliance/test measurement load in place of any real PCI Express interconnect + RX component.
- There are two eye diagrams that must be met for the Transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.
- The eye diagram must be valid for any 250 consecutive UIs.
- A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

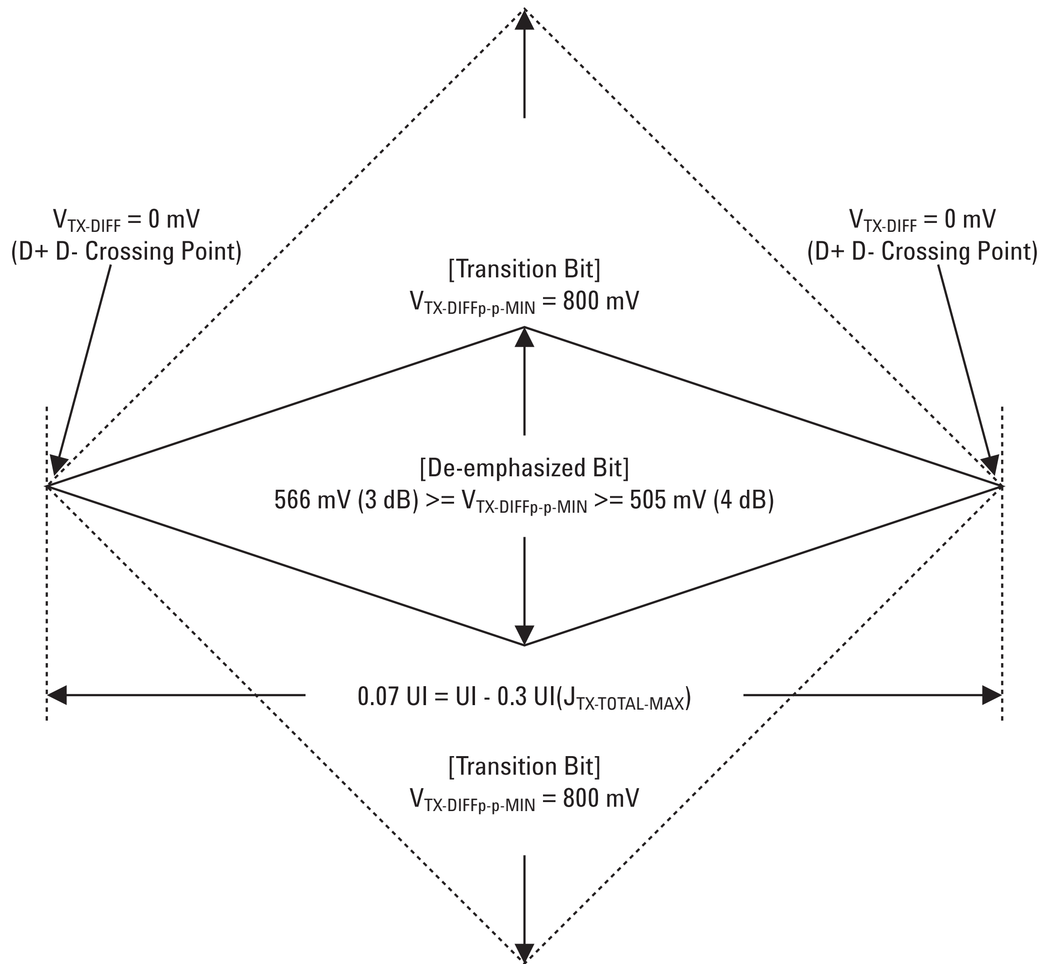


Figure 7 Minimum Transmitter Timing and Voltage Output Compliance Specification.

Test References

Table 4 Template Tests Test References

Test Name	Reference	PCI-SIG Assertions
Template Tests	PCI Express Base Specification, Rev 1.0a, Section 4.3.3.1, Figure 4-26	PHY.3.3#1

Tx, Median to Max Jitter

Table 5 $T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ from Table 4-5 of the Base Specification.

Symbol	Parameter	Min	Nom	Max
$T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	Maximum time between the jitter median and maximum deviation from the median.			0.15 UI

Test Definition Notes from the Specification

- Jitter is defined as the measurement variation of the crossing points ($V_{TX\text{-}DIFFp\text{-}p}$ = 0 V) in relation to the recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used to calculate the TX UI.
- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured over any 250 consecutive TX UIs. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).
- A $T_{TX\text{-}EYE}$ = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX\text{-}JITTER\text{-}MAX}$ = 0.30 UI for the Transmitter collected over any 250 consecutive TX UIs. The $T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs.

  It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
- $T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ (Maximum time between the jitter median and maximum deviation from the median.) is defined in Table 4-5 (Base Specification).

Limits

Maximum = 0.15 UI

Pass Condition

0.15 UI > $T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$

Test Procedure

Follow the procedure in “Running Signal Quality Tests" on page 34, and select “Median to Max Jitter”.

Measurement Algorithm

This measurement is made over 250 consecutive bits defined in Section 3.4 (Base Specification).

The measured time difference between a data edge and a recovered clock edge.

$$tie(n) = t_{R\text{-}DAT}(n) - t_{DAT}(n)$$

Where:

t_{DAT} is the original data edge.

$t_{R\text{-}DAT}$ is the recovered data edge (the ideal time of the data edge as defined by the recovered clock around t_{DAT}).

n is the index of all edges in the waveform.

Test References

Table 6 Median to Max Jitter Test References

Test Name	Reference	PCI-SIG Assertions
Median to Max Jitter	PCI Express Base Specification, Rev 1.0a, Table 4-5	PHY.3.3#4

Tx, Eye-Width

Table 7 $T_{TX\text{-}EYE}$ from Table 4-5 of the Base Specification.

Symbol	Parameter	Min	Nom	Max
$T_{TX\text{-}EYE}$	Minimum TX Eye Width	0.70 UI		

Test Definition Notes from the Specification

- The maximum Transmitter jitter can be derived as $T_{TX\text{-}MAX\text{-}JITTER} = 1 - T_{TX\text{-}EYE} = 0.3$ UI.

- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured over any 250 consecutive TX UIs. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).
- A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the Transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs.

NOTE The median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

- T_{TX-EYE} (Minimum TX Eye Width) is defined in Table 4-5 (Base Specification).

Limits

Minimum = 0.70 UI and the Pass Condition is 0.70 UI < T_{TX-EYE}.

Test Procedure

Follow the procedure in “Running Signal Quality Tests" on page 34, and select “Eye-Width”.

Measurement Algorithm

This measurement is made over 250 consecutive bits defined in Section 3.4 (Base Specification).

The measured minimum horizontal eye opening at the zero reference level as shown in the eye diagram.

$$T_{EYE-WIDTH} = UI_{AVG} - TIE_{Pk-Pk}$$

Where:

UI_{AVG} is the average UI.

TIE_{Pk-Pk} is the Peak-Peak TIE.

Test References

Table 8 Eye-Width Test References

Test Name	Reference	PCI-SIG Assertions
Eye-Width	PCI Express Base Specification, Rev 1.0a, Table 4-5	PHY.3.3#9

Tx, Peak Differential Output Voltage

Table 9 $V_{TX\text{-}DIFFp\text{-}p}$ from Table 4-5 of the Base Specification.

Symbol	Parameter	Min	Nom	Max
$V_{TX\text{-}DIFFp\text{-}p}$	Differential Pk-Pk Output Voltage	0.80 V		1.2 V

Test Definition Notes from the Specification

- $V_{TX\text{-}DIFFp\text{-}p} = 2^*|V_{TX\text{-}D+} - V_{TX\text{-}D-}|$
- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured over any 250 consecutive TX UIs. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).

Test Procedure

Follow the procedure in “Running Signal Quality Tests" on page 34, and select “Peak Differential Output Voltage”.

PASS Condition

$0.8 \text{ V} <= V_{TX\text{-}DIFF\text{-}p\text{-}p} <= 1.2\text{V}$

Measurement Algorithm

The Differential Peak Voltage measurement returns two times the larger of the Min or Max statistic of the differential voltage waveform.

$$V_{TX\text{-}DIFF\text{-}p\text{-}p} = 2^*\text{Max}(\ \text{Max}(V_{DIFF(i)}),\ \text{Min}(V_{DIFF(i)}))$$

Where:

i is the index of all waveform values.

V_{DIFF} is the Differential Voltage signal.

Test References

Table 10 Peak Differential Output Voltage Test References

Test Name	Reference	PCI-SIG Assertions
Peak Differential Output Voltage	PCI Express Base Specification, Rev 1.0a, Table 4-5	PHY.3.2#2

Tx, Rise/Fall Time

Table 11 $T_{TX\text{-}RISE}$, $T_{TX\text{-}FALL}$ from Table 4-5 of the Base Specification.

Symbol	Parameter	Min	Nom	Max
$T_{TX\text{-}RISE}$, $T_{TX\text{-}FALL}$	D+/D- TX Output Rise/Fall Time	0.125UI		

Test Definition Notes from the Specification

- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured over any 250 consecutive TX UIs. Also refer to the Transmitter compliance (Base Specification).
- Measured between 20-80% at Transmitter package pins into a test load as shown in Figure 4-25 for both $V_{TX\text{-}D+}$ and $V_{TX\text{-}D-}$.
- $T_{TX\text{-}RISE}$, $T_{TX\text{-}FALL}$ (D+/D- TX Output Rise/Fall Time) is defined in Table 4-5 (Base Specification).

Limits

Minimum = 0.125 UI and the Pass Condition is 0.125 UI < $T_{TX\text{-}RISE}$, $T_{TX\text{-}FALL}$.

Test Procedure

Follow the procedure in “Running Signal Quality Tests" on page 34, and select “Rise/Fall Time”.

Measurement Algorithms

Rise/Fall time is limited to only rising or falling edges of consecutive transitions for transmitter measurements. Rise/Fall Time is taken independently on each single ended waveform sources when you use two single ended probes or two SMA cables as the signal source. Differential signal Rise/Fall Time show up when you select Differential probe type.

Rise Time. The Rise Time measurement is the time difference between when the VREF-HI reference level is crossed and the VREF-LO reference level is crossed on the rising edge of the waveform.

$t_{RISE}(n) = t_{HI+}(i) - t_{LO+}(j)$

Where:

t_{RISE} is a Rise Time measurement.

t_{HI+} is a set of t_{HI} for rising edges only.

t_{LO+} is a set of t_{LO} for rising edges only.

i and j are indexes for nearest adjacent pairs of t_{LO+} and t_{HI+}.

n is the index of rising edges in the waveform.

Rise Time for $v_{D+}(t)$ is as follows:

$t_{D+RISE}(n) = t_{D+HI+}(i) - t_{D+LO+}(j)$

and for $v_{D-}(t)$:

$t_{D-FALL}(n) = t_{D-LO-}(i) - t_{D-HI-}(j)$

Fall Time. The Fall Time measurement is the time difference between when the VREF-HI reference level is crossed and the VREF-LO reference level is crossed on the falling edge of the waveform.

$t_{FALL}(n) = t_{LO-}(i) - t_{HI-}(j)$

Where:

t_{FALL} is a Fall Time measurement.

t_{HI-} is set of t_{HI} for falling edge only.

t_{LO-} is set of t_{LO} for falling edge only.

i and j are indexes for nearest adjacent pairs of t_{LO-} and t_{HI-}.

n is the index of falling edges in the waveform.

Fall Time for $v_{D+}(t)$ is as follows:

$t_{D+FALL}(n) = t_{D+LO-}(i) - t_{D+HI-}(j)$

and for $v_{D-}(t)$:

$t_{D-FALL}(n) = t_{D-LO-}(i) - t_{D-HI-}(j)$

Test References

Table 12 Rise/Falltime Test References

Test Name	Reference	PCI-SIG Assertions
Rise/Falltime	PCI Express Base Specification, Rev 1.0a, Table 4-5	PHY.3.3#3

Tx, Deemphasized Voltage Ratio

Table 13 $V_{TX\text{-}DE\text{-}RATIO}$ from Table 4-5 of the Base Specification.

Symbol	Parameter	Min	Nom	Max
$V_{TX\text{-}DE\text{-}RATIO}$	De-Emphasized Differential Output Voltage (Ratio)	-3.0 dB	-3.5 dB	-4.0 dB

Test Definition Notes from the Specification

- This is the ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition.
- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) in the serial data standard and measured over any 250 consecutive TX UIs. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).
- $V_{TX\text{-}DE\text{-}RATIO}$ (De-Emphasized Differential Output Voltage (Ratio)) is defined in Table 4-5 (Base Specification).

Limits

Minimum = -4.0 dB and Maximum = -3.0 dB, and the Pass Condition is $-4.0\ dB < V_{TX\text{-}DE\text{-}RATIO} < -3.0\ dB$.

Test Procedure

Follow the procedure in “Running Signal Quality Tests" on page 34, and select “Deemphasized Voltage Ratio”.

Measurement Algorithm

This measurement is made over 250 consecutive bits defined in Section 3.4 (Base Specification).

The De-Emphasis measurement calculates the ratio of any non-transition eye voltage (2nd, 3rd, etc. eye voltage succeeding an edge) to its nearest preceding transition eye voltage (1st eye voltage succeeding an edge). In Figure 7, it is the ratio of the black voltages over the blue voltages. The results are given in dB.

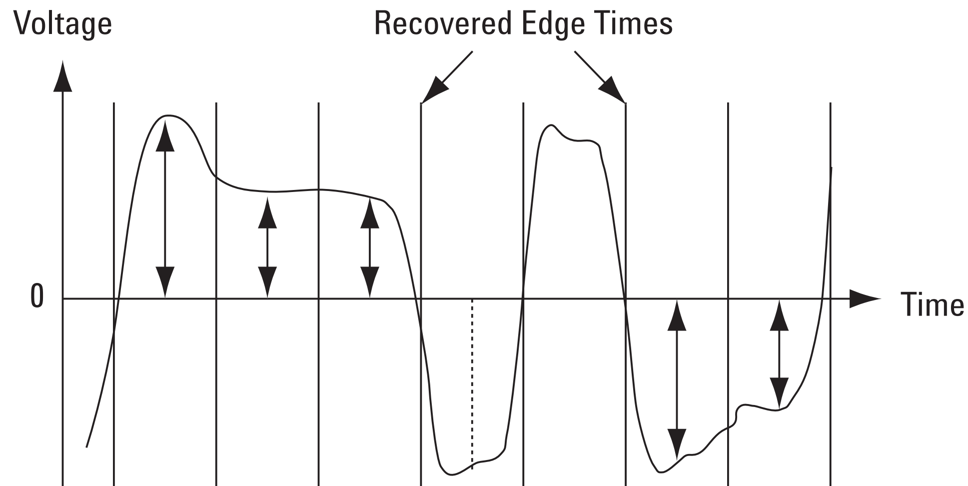


Figure 8 DeEmphasis Measurement.

$$\mathrm{DEEM}(m) = dB\left(\frac{v_{\mathrm{EYE\text{-}HI\text{-}NTRAN}}(m)}{v_{\mathrm{EYE\text{-}HI\text{-}TRAN}}(n)}\right)$$

or

$$\mathrm{DEEM}(m) = dB\left(\frac{v_{\mathrm{EYE\text{-}LO\text{-}NTRAN}}(m)}{v_{\mathrm{EYE\text{-}LO\text{-}TRAN}}(n)}\right)$$

Where:

$v_{EYE-HI-TRAN}$ is the High voltage at mid UI following a positive transition.

$v_{EYE-LO-TRAN}$ is the Low voltage at mid UI following a negative transition.

$v_{EYE-HI-NTRAN}$ is the High voltage at mid UI following a positive transition bit.

$v_{EYE-LO-NTRAN}$ is the Low voltage at mid UI following a negative transition bit.

m is the index for all non-transition UIs.

n is the index for the nearest transition UI preceding the UI specified by m.

Test References

Table 14 Deemphasized Voltage Ratio Test References

Test Name	Reference	PCI-SIG Assertions
Deemphasized Voltage Ratio	PCI Express Base Specification, Rev 1.0a, Table 4-5	PHY.3.2#1

Running Common Mode Voltage Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 22. Then, when selecting tests, navigate to "Common Mode Voltage" in the "Transmitter (Tx) Tests" group.

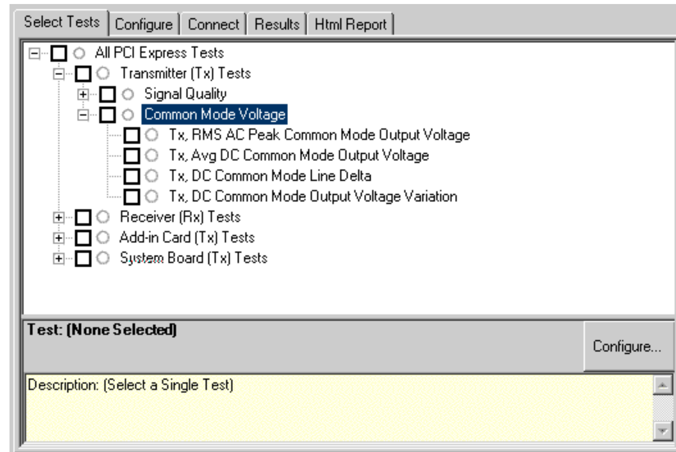


Figure 9 Selecting Transmitter (Tx) Common Mode Voltage Tests

Tx, RMS AC Peak Common Mode Output Voltage

Table 15 $V_{TX\text{-}CM\text{-}ACp}$ from Table 4-5 of the Base Specification.

Symbol	Parameter	Min	Nom	Max
$V_{TX\text{-}CM\text{-}ACp}$	RMS AC Peak Common Mode Output Voltage			20 mV

Test Definition Notes from the Specification

$V_{TX-CM-ACp} = RMS(|V_{TX-D+} + V_{TX-D-}| \div 2 - V_{TX-CM-DC}) V_{TX-CM-DC} = DC_{(avg)}$ of $|V_{TX-D+} + V_{TX-D-}| \div 2$

- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured over any 250 consecutive TX UIs. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).
- $V_{TX-CM-ACp}$ (RMS AC Pk Common Mode Output Voltage) is defined in Table 4-5 (Base Specification).

Limits

Maximum = 20 mV and the Pass Condition is 20 mV > $V_{TX-CM-ACp}$.

Test Procedure

Follow the procedure in “Running Common Mode Voltage Tests" on page 46, and select “RMS AC Peak Common Mode Output Voltage”.

NOTE

This test is only available when the single-ended or SMA probing method has been used (see “Probing the Link for Tx Compliance" on page 30).

Measurement Algorithm

AC CM RMS Voltage. The AC Common Mode RMS Voltage measurement calculates the RMS statistic of the Common Mode voltage waveform with the DC Value removed.

$$v_{AC-RMS-CM}(i) = RMS(v_{AC-M}(i))$$

Where:

i is the index of all waveform values.

$v_{AC-RMS-CM}$ is the RMS of the AC Common Mode voltage signal.

v_{AC-M} is the AC Common Mode voltage signal.

Test References

Table 16 RMS AC Peak Common Mode Output Voltage Test References

Test Name	Reference	PCI-SIG Assertions
RMS AC Peak Common Mode Output Voltage	PCI Express Base Specification, Rev 1.0a, Table 4-5	PHY.3.3#5

Tx, Avg DC Common Mode Output Voltage

Table 17 $V_{TX\text{-}DC\text{-}CM}$ from Table 4-5 of the Base Specification.

Symbol	Parameter	Min	Nom	Max
$V_{TX\text{-}DC\text{-}CM}$	The TX DC Common Mode Voltage	0 V		3.6 V

Test Definition Notes from the Specification

The TX DC common mode voltage ($V_{TX\text{-}DC\text{-}CM}$) must be held at the same value during all states. The allowable range for $V_{TX\text{-}DC\text{-}CM}$ is 0 to 3.6 V (+/- 100mV).

Limits

$0 \text{ V} <= V_{TX\text{-}DC\text{-}CM} <= 3.6 \text{ V}$

Test Procedure

Follow the procedure in "Running Common Mode Voltage Tests" on page 46, and select "Avg DC Common Mode Output Voltage".

NOTE This test is only available when the single-ended or SMA probing method has been used (see "Probing the Link for Tx Compliance" on page 30).

Measurement Algorithm

The Avg DC Common Mode Voltage measurement computes the DC average of the common mode signal:

$$V_{TX\text{-}DC\text{-}CM} = DC_{(avg)} \text{ of } |V_{TX\text{-}D+} + V_{TX\text{-}D-}|/2$$

NOTE The base specification states that $V_{TX\text{-}DC\text{-}CM}$ must be held at the same value during all states. For complete validation, this measurement should be performed on the device in all states and the results compared.

Test References

Table 18 Avg DC Common Mode Output Voltage Test References

Test Name	Reference	PCI-SIG Assertions
Avg DC Common Mode Output Voltage	PCI Express Base Specification, Rev 1.0a, Table 4-5	PHY.3.1#12

Tx, DC Common Mode Line Delta

Table 19 $V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$ from Table 4-5 of the Base Specification

Symbol	Parameter	Min	Nom	Max
$V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0 V		25 mV

Test Definition Notes from the Specification

$|V_{TX\text{-}CM\text{-}DC\text{-}D+} - V_{TX\text{-}CM\text{-}DC\text{-}D-}| \leq 25$ mV, $V_{TX\text{-}CM\text{-}DC\text{-}D+} = DC_{(avg)}$ of $|V_{TX\text{-}D+}|$, $V_{TX\text{-}CM\text{-}DC\text{-}D-} = DC_{(avg)}$ of $|V_{TX\text{-}D-}|$

- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured over any 250 consecutive TX UIs. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).
- $V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$ (Absolute Delta of DC Common Mode Voltage between D+ and D-) Is defined in Table 4-5 (Base Specification).

Limits

$V_{TX\text{-}CM\text{-}LINE\text{-}DELTA} < 25mV$

Test Procedure

Follow the procedure in “Running Common Mode Voltage Tests" on page 46, and select “DC Common Mode Line Delta”.

NOTE This test is only available when the single-ended or SMA probing method has been used (see “Probing the Link for Tx Compliance" on page 30).

Measurement Algorithm

$V_{TX-CM-LINE-DELTA}$ is computed as the absolute value of the difference between the DC average of V_{TX-D+} and the DC average of V_{TX-D-}

$$V_{TX-CM-LINE-DELTA} = |V_{TX-CM-DC+} - V_{TX-CM-DC-D-}|$$

Where:

$V_{TX-CM-DC+}$ is the $DC_{(avg)}$ of V_{TX-D+}

$V_{TX-CM-DC-}$ is the $DC_{(avg)}$ of V_{TX-D-}

Test References

Table 20 DC Common Mode Line Delta Test References

Test Name	Reference	PCI-SIG Assertions
DC Common Mode Line Delta	PCI Express Base Specification, Rev 1.0a, Table 4-5	PHY.3.1#26

Tx, DC Common Mode Output Voltage Variation

Test Definition Notes from the Specification

The TX DC common mode voltage ($V_{TX-DC-CM}$) must be held at the same value during all states. The allowable range for $V_{TX-DC-CM}$ is 0 to 3.6 V (+/- 100mV).

Limits

$|V_{TX-DC-CM-VARIATION}| <= 100$ mV

Test Procedure

Follow the procedure in “Running Common Mode Voltage Tests" on page 46, and select “DC Common Mode Output Voltage Variation”.

NOTE This test is only available when the single-ended or SMA probing method has been used (see “Probing the Link for Tx Compliance" on page 30).

Measurement Algorithm

The Tx DC Common Mode Output Voltage Variation measurement computes the worst case positive or negative excursion of the common mode signal from the average DC Common Mode Voltage $V_{TX-DC-CM}$

$V_{TX-DC-CM-VARIATION} = | Max(Max(V_{CM(i)}), Min(V_{CM(i)})) - V_{TX-DC-CM} |$

Where:

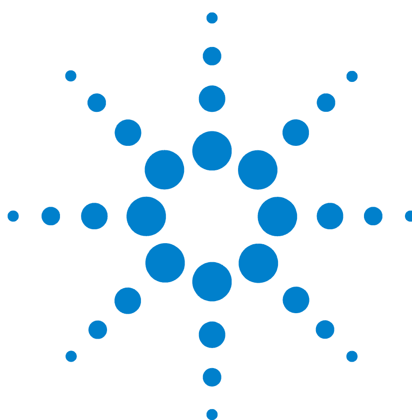
i is the index of all waveform values.

V_{CM} is the common mode signal $(V_{TX-D+} + V_{TX-D-})/2$.

Test References

Table 21 DC Common Mode Output Voltage Variation Test References

Test Name	Reference	PCI-SIG Assertions
DC Common Mode Output Voltage Variation	PHY ELECTRICAL TEST CONSIDERATIONS, REVISION 1.0RD, Section 4.1.6	PHY.3.1#12



3
Transmitter (Tx) Tests, PCI-E 1.0a, Low Power

Probing the Link for Tx Compliance 55
Tx Compliance Test Load 55
Running Signal Quality Tests 55
Running Common Mode Voltage Tests 58

This section provides the Methods of Implementation (MOIs) for Transmitter tests using an Agilent 54855A, 80000B, or 90000A series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

The *Mobile Graphic Low Power Addendum to The PCIE Base Specification 1.0* describes the reduced power requirement of a transmitter on Mobile Platform. To meet low power requirement, a device must be compliant to the PCIE Base Specfication 1.0a except for electrical specification in section 2.2 of the addendum. The addendum also states that a low power device does not implement de-emphasis.

PCIE 1.0a Low Power Transmitter Tests consist of all tests from PCIE 1.0 Full (Standard) Power Tests except de-emphasis tests. The following table shows all the PCIE 1.0a Low Power Tests:

Table 22 PCIE 1.0a Low Power Transmitter Tests

Test Name	Remarks	See
Unit Interval	Same as Full Power	page 35.
Template Tests	Different	page 56.
Median to Max Jitter	Different	page 57.
Eye-Width	Different	page 57.
Peak Differential Output Voltage	Different	page 57.
Rise/Fall Time	Same as Full Power	page 42.
RMS AC Peak Common Mode Output Voltage	Same as Full Power	page 46.
Avg DC Common Mode Output Voltage	Same as Full Power	page 48.
DC Common Mode Output Voltage Variation	Same as Full Power	page 50.
DC Common Mode Line Delta	Same as Full Power	page 49.

All the tests above remarked with “Same as Full Power” share the same Method of Implementation (MOI) with PCIE 1.0 Full Power (refer to the page numbers shown). The differences in the test method are described in this chapter.

Probing the Link for Tx Compliance

When performing low-power transmitter tests, probing is the same as for full-power tests. See "Probing the Link for Tx Compliance" on page 30.

Tx Compliance Test Load

When performing low-power transmitter tests, the compliance test load is the same as for full-power tests. See "Tx Compliance Test Load" on page 34.

Running Signal Quality Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 22. Then, when selecting tests, navigate to "Signal Quality" in the "Transmitter (Tx) Tests" group.

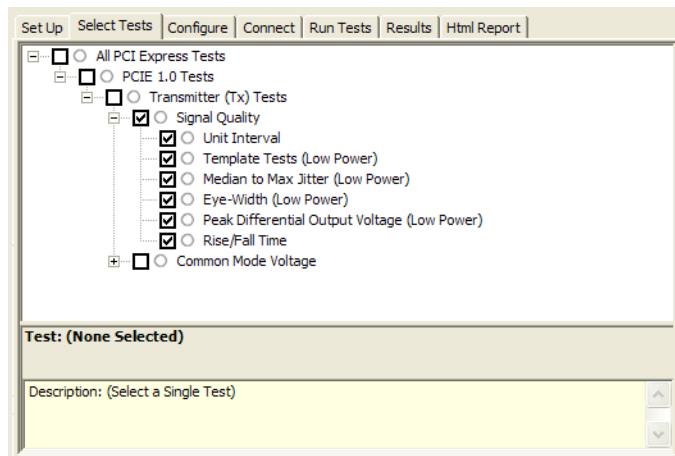


Figure 10 Selecting Transmitter (Tx) Signal Quality Tests

Tx, Unit Interval

When performing low-power transmitter tests, the Tx Unit Interval test is the same as for full-power tests. See "Tx, Unit Interval" on page 35.

Tx, Template Tests (Low Power)

Test Definition/Reference

Mobile Graphics Low-Power Addendum to the PCI Express Base Specification 1.0

- Compliance of the transmitter eye diagram uses the same methodology as outlined in PCI Express Base 1.0a. The Tx eye diagram is specified using the passive compliance/test measurement load (see Figure 2-1 of Mobile Low Power PCIE Specification) in place of any real PCI Express interconnect plus Rx component. Because de-emphasis is not implemented, the transition and de-emphasized bit transitions are merged into a single Transmitter compliance eye diagram.
- The eye diagram must be valid for any 250 consecutive UIs.
- A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

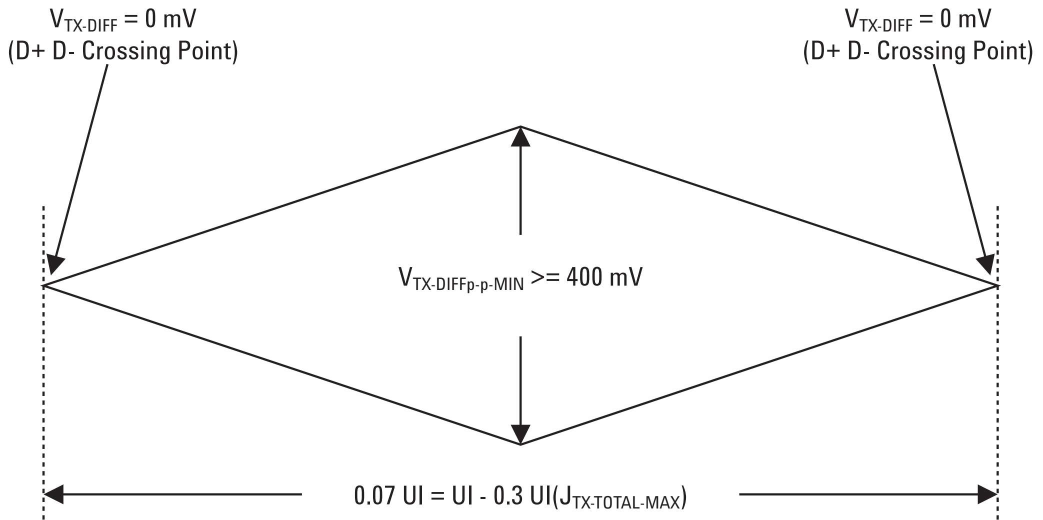


Figure 11 Transmitter Compliance Eye Diagram from Figure 2-2 of the Mobile Graphic Low-Power Addendum.

Difference in Test Procedure Compared to Full Power

- Different Eye diagram used. The Eye diagram can be found in Figure 2.2 of Mobile Low Power PCIE Specification.
- Eye diagram only runs once with both transition and non-transition bits since de-emphasis is no longer needed for low power specification.

See Also "Tx, Template Tests" on page 36.

Tx, Median to Max Jitter (Low Power)

Difference in Test Procedure Compared to Full Power

- Eye diagram only runs once with both transition and non-transition bits since de-emphasis is no longer needed for low power specification.

See Also “Tx, Median to Max Jitter" on page 38.

Tx, Eye-Width (Low Power)

Difference in Test Procedure Compared to Full Power

- Eye diagram only runs once with both transition and non-transition bits since de-emphasis is no longer needed for low power specification.

See Also “Tx, Eye-Width" on page 39.

Tx, Peak Differential Output Voltage (Low Power)

Difference in Test Procedure Compared to Full Power

- Different specification used:

Table 23 $V_{TX-DIFFp-p}$ from Table 2-1 of the Mobile Graphic Low-Power Addendum.

Symbol	Parameter	Min	Nom	Max
$V_{TX-DIFFp-p}$	Differential Pk-Pk Output Voltage	0.400 V		1.2 V

- $V_{TX-DIFFp-p} = 2*|V_{TX-D+} - V_{TX-D-}|$
- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 2-1 (Mobile Graphic Low Power Addemdum) and measured over any 250 consecutive TX UIs. Also refer to the Transmitter compliance eye diagram shown in Figure 2-2 (Mobile Graphic Low Power Addemdum).

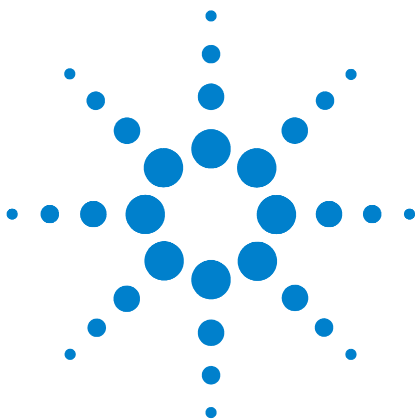
See Also “Tx, Peak Differential Output Voltage" on page 41.

Tx, Rise/Fall Time

When performing low-power transmitter tests, the Tx Rise/Fall Time test is the same as for full-power tests. See “Tx, Rise/Fall Time" on page 42.

Running Common Mode Voltage Tests

When performing low-power transmitter tests, the common mode voltage tests are the same as for full-power tests. See "Running Common Mode Voltage Tests" on page 46.



4
Receiver (Rx) Tests, PCI-E 1.0a

Probing the Link for Rx Compliance 60
Running Receiver Tests 63

This section provides the Methods of Implementation (MOIs) for Receiver tests using an Agilent 54855A, 80000B, or 90000A series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

NOTE

None of the included receiver tests validate the receiver's ability to correctly receive data (also known as receiver tolerance). Rather, they validate that the signal as seen by the reciever meets or exceeds various parameters (maximum voltage, jitter, eye width, etc.). These tests validate the transmitter and interconnect. Separate reciever tolerance testing is required to ensure the receiver is correctly receiving data.

Probing the Link for Rx Compliance

Receiver tests are done by probing the link as close as is feasibly possible to the pins of the receiver device. Alternatively, a dummy load can be used for the termination of the link. To probe the receiver link, you can:

- Use two differential probe heads with two 1134A probe amplifiers (with the negative lead grounded for single-ended measurements) and the Ch1 and Ch3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.
- Use one differential probe head with the 1134A probe amplifier and the Ch2 input of an oscilloscope that has 20 GS/s sample rate available on that channel.

Table 24 Probing Options for Receiver Testing

	Probing Configurations			**Captured Waveforms**		**System Specifications**	
						54855A	
	Probing Method	**Break Serial Link**	**Channels Used**	**Differential Mode**	**Common Mode**	**System Band Width**	**Rise* Time (20-80)**
DUT Connection	Single-Ended (2 x 1134A w/ Differential Probe Heads)	Y/N	2	Pseudo	Yes	6 GHz	70 ps
	Differential (1 x 1134A w/ Differential Probe Head)	Y/N	1	True	No	6 GHz	70 ps

*Typical

Single-Ended Probing (Ch1) and (Ch3)

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Ch1-Ch3. The Common mode measurements are also available in this configuration from the common mode waveform (Ch1+Ch3)/2.

Make sure to probe equal distances from the receiver, as close as possible to the receiver, with the shortest ground connection possible.

This probing technique can be used for either a live link that is transmitting data, or a link terminated into a "dummy load."

Channel-to-channel deskew is required using this technique because two channels are used.

For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, "InfiniiMax Probing Options," starting on page 392.

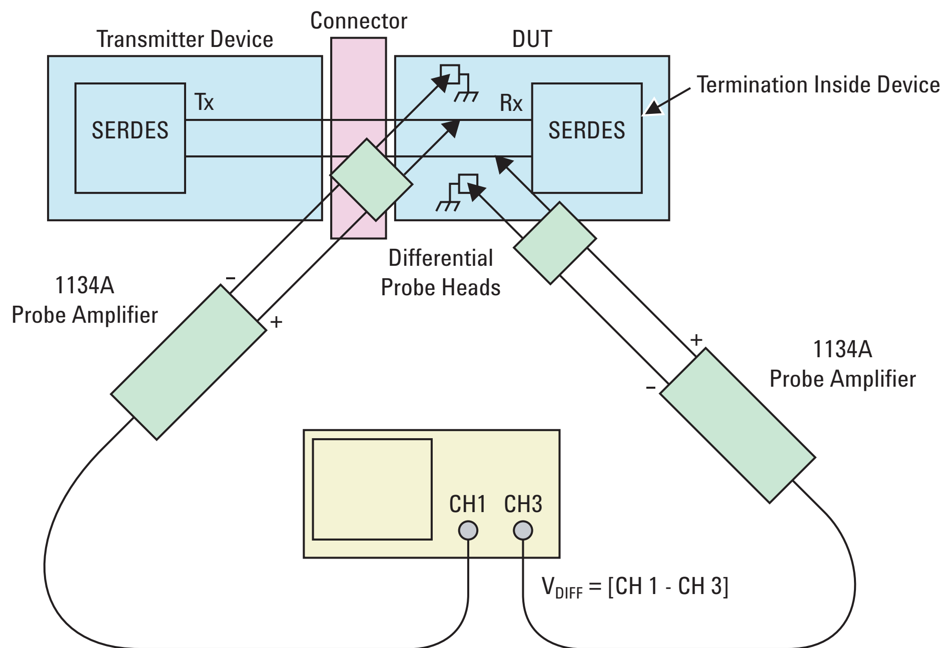


Figure 12 Single-Ended Probing

Differential Probing (Ch2)

The differential signal is measured directly by the differential probe head.

Make sure to probe equal distances from the receiver, as close as possible to the receiver, with the shortest ground connection possible.

This probing technique can be used for either a live link that is transmitting data, or a link terminated into a "dummy load."

A single channel of the oscilloscope is used, so de-skew is not necessary.

For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, "InfiniiMax Probing Options," starting on page 392.

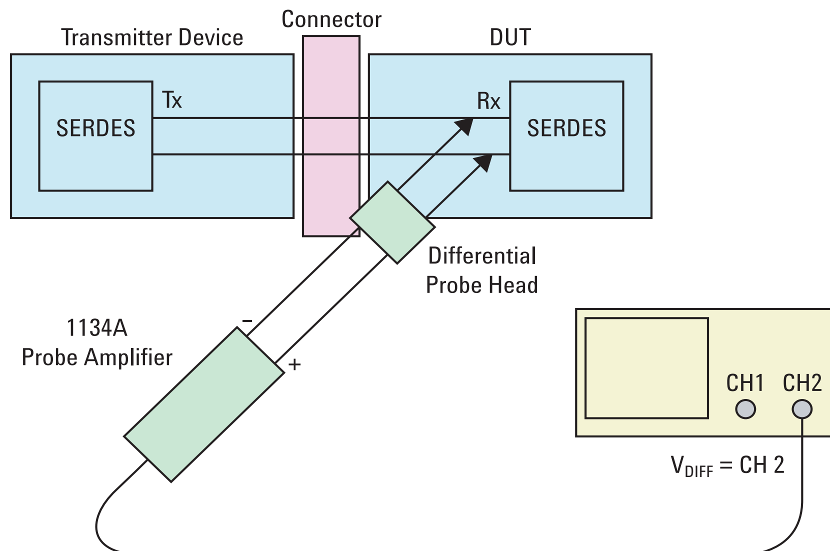


Figure 13 Differential Probing

Running Receiver Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 22. Then, when selecting tests, navigate to the "Receiver (Rx) Tests" group.

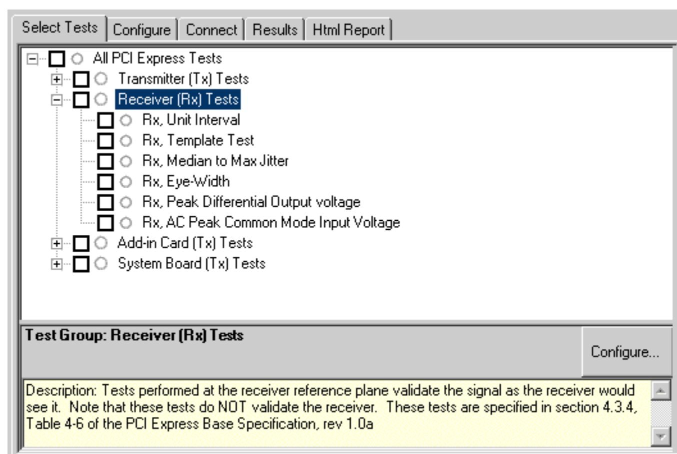


Figure 14 Selecting Receiver (Rx) Tests

Unit Interval

Table 25 UI from Table 4-6 of the Base Specification

Symbol	Parameter	Min	Nom	Max
UI	Unit Interval	399.88 ps	400ps	400.12 ps

Refer to "Tx, Unit Interval" on page 35. The MOI for the measurement of UI at the receiver is identical to measuring it at the transmitter, with the exception of the test point.

Test References

Table 26 Unit Interval Test References

Test Name	Reference	PCI-SIG Assertions
Unit Interval	PCI Express Base Specification, Rev 1.0a, Table 4-6	

Template Test

See Section 4.3.4 of the Base Specification for additional notes and test definitions.

Test Definition Notes from the Specification

- The RX eye diagram in Figure 4-26 (Base Specification) is specified using the passive compliance/test measurement load (see Figure 4-25, Base Specification) in place of any real PCI Express RX component.

NOTE

In general, the minimum Receiver eye diagram measured with the compliance/test measurement load (see Figure 4-25, Base Specification) will be larger than the minimum Receiver eye diagram measured over a range of systems at the input Receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input Receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 4-26, Base Specification) expected at the input Receiver based on some adequate combination of system simulations and the Return Loss measured looking into the RX package and silicon.

- The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.
- The eye diagram must be valid for any 250 consecutive UIs.
- A recovered RX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the RX UI.

Test Procedure

Follow the procedure in “Running Receiver Tests" on page 63, and select “Template Test”.

Measurement Algorithm

This measurement is made over 250 consecutive bits defined in Section 3.4 (Base Specification).

The acquisition points are compared to the mask geometry (defined in Figure 4.24, Base Specification) and mask collisions are reported as Mask Hits in the Measurement Results Area.

If Mask Hits > 0, then a Failure is indicated in the Results tab.

Test References

Table 27 Template Test Test References

Test Name	Reference	PCI-SIG Assertions
Template Test	PCI Express Base Specification, Rev 1.0a, Figure 4-26	PHY.3.4#1

Median to Max Jitter

Table 28 $T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ from Table 4-6 of the Base Specification

Symbol	Parameter	Min	Nom	Max
$T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	Maximum time between the jitter median and maximum deviation from the median.			0.3 UI

Test Definition Notes from the Specification

- Jitter is defined as the measurement variation of the crossing points ($V_{RX\text{-}DIFFp\text{-}p}$ = 0 V) in relation to a recovered RX UI. A recovered RX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the RX UI.
- Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 4-25 (Base Specification) should be used as the RX device when taking measurements. Also refer to the Receiver compliance eye diagram shown in Figure 4-26 (Base Specification). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
- A $T_{RX\text{-}EYE}$ = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total 0.6 UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.

- $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ (Maximum time between the jitter median and maximum deviation from the median) is defined in Table 4-6 (Base Specification).

Limits

Maximum = 0.30 UI and the Pass Condition is $0.3UI > T_{RX-EYE-MEDIAN-to-MAX-JITTER}$.

Test Procedure

Follow the procedure in “Running Receiver Tests" on page 63, and select “Median to Max Jitter”.

Measurement Algorithm

Refer to “Tx, Median to Max Jitter" on page 38 for Rx Median-to-Max Jitter measurement algorithm.

Test References

Table 29 Median to Max Jitter Test References

Test Name	Reference	PCI-SIG Assertions
Median to Max Jitter	PCI Express Base Specification, Rev 1.0a, Table 4-6	PHY.3.4#6

Eye-Width

Table 30 T_{RX-EYE} from Table 4-6 of the Base Specification

Symbol	Parameter	Min	Nom	Max
T_{RX-EYE}	Minimum Receiver Eye Width	0.4 UI		

Test Definition Notes from the Base Specification

- The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI.

- Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 4-25 (Base Specification) should be used as the RX device when taking measurements. Also refer to the Receiver compliance eye diagram shown in Figure 4-26 (Base Specification). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
- A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected over any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total .6 UI jitter budget collected over any 250 consecutive TX UIs.

NOTE

The median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.

- T_{RX-EYE} (Minimum RX Eye Width) is defined in Table 4-6 of Version 1.0a of the Base Specification.

Limits

Minimum = 0.40 UI and the Pass Condition is 0.40UI < T_{RX-EYE}.

Test Procedure

Follow the procedure in “Running Receiver Tests" on page 63, and select “Eye-Width”.

Measurement Algorithm

Refer to “Tx, Eye-Width" on page 39 for Eye Width measurement algorithm.

Test References

Table 31 Eye-Width Test References

Test Name	Reference	PCI-SIG Assertions
Eye-Width	PCI Express Base Specification, Rev 1.0a, Table 4-6	PHY.3.4#1

Peak Differential Output Voltage

Table 32 $T_{RX\text{-}DIFFp\text{-}p}$ from Table 4-6 of the Base Specification

Symbol	Parameter	Min	Nom	Max
$V_{RX\text{-}DIFFp\text{-}p}$	Differential Input Peak to Peak Voltage	0.175 V		1.2 V

Test Definition Notes from the Specification

- $V_{RX\text{-}DIFFp\text{-}p} = 2^*|V_{RX\text{-}D+} - V_{RX\text{-}D-}|$
- Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 4-25 (Base Specification) should be used as the RX device when taking measurements. Also refer to the Receiver compliance eye diagram shown in Figure 4-26 (Base Specification). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
- $V_{RX\text{-}DIFFp\text{-}p}$ (Differential Input Pk-Pk Voltage) is defined in Table 4-6 (Base Specification). Differential Pk-Pk Voltage Characteristics.(Maximum = 1.2 V and Minimum = 0.175 V). This measurement is solved by 2 measurements. One is Differential Peak Voltage the other one is Eye Height measurement.

Test Procedure

Follow the procedure in “Running Receiver Tests" on page 63, and select “Peak Differential Output Voltage”.

PASS Condition

$V_{RX\text{-}DIFFp\text{-}p} < 1.2$ V and 0.175 V < Eye Height

Measurement Algorithm

Refer to “Tx, Peak Differential Output Voltage" on page 41 for Differential Voltage measurement algorithms.

NOTE For receiver testing, Eye Height is measured on all UIs.

Test References

Table 33 Peak Differential Output Voltage Test References

Test Name	Reference	PCI-SIG Assertions
Peak Differential Output Voltage	PCI Express Base Specification, Rev 1.0a, Table 4-6	PHY.3.4#1

AC Peak Common Mode Input Voltage

Table 34 $V_{RX\text{-}CM\text{-}ACp}$ from Table 4-6 of the Base Specification

Symbol	Parameter	Min	Nom	Max
$V_{RX\text{-}CM\text{-}ACp}$	AC Peak Common Mode Input Voltage			150 mV

Test Definition Notes from Specification

- $V_{RX\text{-}CM\text{-}AC} = |V_{RX\text{-}D+} + V_{RX\text{-}D-}| \div 2 - V_{RX\text{-}CM\text{-}DC}$

  $V_{RX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $|V_{RX\text{-}D+} + V_{RX\text{-}D-}| \div 2$
- Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 4-25 (Base Specification) should be used as the RX device when taking measurements. Also refer to the Receiver compliance eye diagram shown in Figure 4-26 (Base Specification). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
- $V_{RX\text{-}CM\text{-}ACp}$ (AC Peak Common Mode Input Voltage) is defined in Table 4-5 (Base Specification).

Limits

Maximum = 150 mV and the Pass Condition is 150 mV > $V_{RX\text{-}CM\text{-}ACp}$.

Test Procedure

Follow the procedure in “Running Receiver Tests" on page 63, and select “AC Peak Common Mode Input Voltage”.

Measurement Algorithms

This measurement is made over 250 consecutive bits defined in Section 3.4 (Base Specification).

AC CM Pk Voltage Measurement. The AC Common Mode Pk Voltage measurement returns the larger of the Min or Max statistic of the Common Mode voltage waveform with the DC Value removed.

$$v_{AC-PK-CM}(i) = Max(Max(v_{AC-M}(i),Min(v_{AC-M}(i))$$

Where:

i is index of all waveform values.

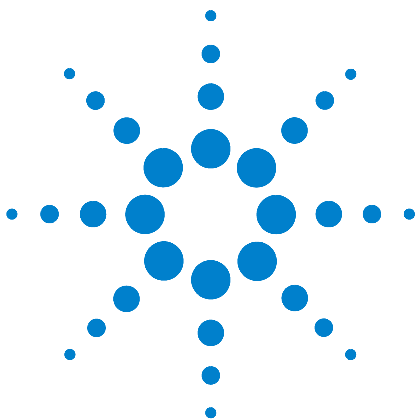
$v_{AC-PK-CM}$ is the Peak of the AC Common Mode voltage signal.

v_{AC-M} is the AC Common Mode voltage signal.

Test References

Table 35 AC Peak Common Mode Input Voltage Test References

Test Name	Reference	PCI-SIG Assertions
AC Peak Common Mode Input Voltage	PCI Express Base Specification, Rev 1.0a, Table 4-6	PHY.3.4#2



5
Add-In Card (Tx) Tests, PCI-E 1.0a

Probing the Link for Add-In Card Compliance 72
Running Add-In Card Tests 75

This section provides the Methods of Implementation (MOIs) for Add-In Card tests using an Agilent 54855A, 80000B, or 90000A Series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

Probing the Link for Add-In Card Compliance

Connecting the Signal Quality Load Board for Add-in Card Testing

There are multiple pairs of SMA connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1 With the Add-in card fixture power supply powered off, connect the power supply connector to the Add-in card test fixture, and connect the device under test add-in card to the by-16 or by-1 connector slot.

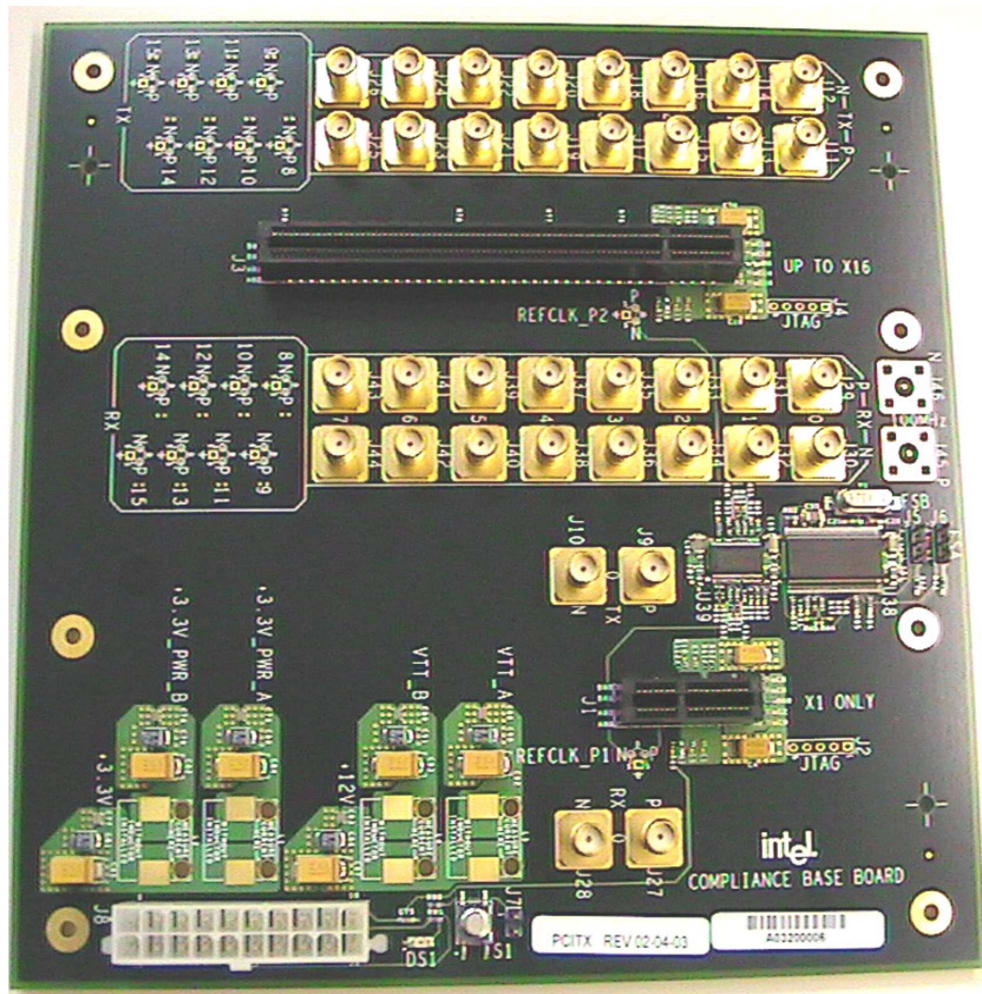


Figure 15 Compliance Base Board (CBB) Add-in Card Fixture

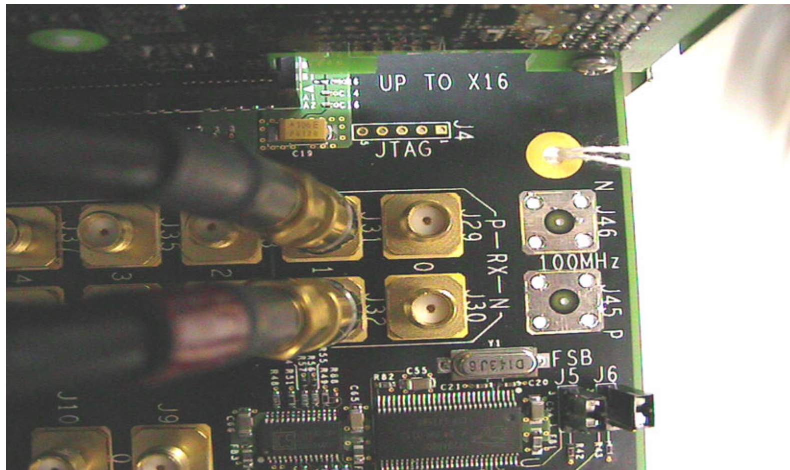


Figure 16 Compliance Base Board (CBB) SMA Probing Option

2 Connect cables up as follows:

a Digital Storage Oscilloscope channel 1 to the TX LANE P under test (where Lane 1 is under test in this example shown in Figure 16 above).

b Digital Storage Oscilloscope channel 3 to the TX LANE N under test (where Lane 1 is under test in this example shown in Figure 16 above).

NOTE The Compliance Base Board labeled PCITX Rev 02-04-03 silkscreen incorrectly labels the add-in card transmitter probing locations as RX.

When SMA probing and two channels are used, channel-to-channel deskew is required (see “Channel-to-Channel De-skew" on page 386).

Not all lanes have SMA probing options. For signal quality testing of the remaining lanes you will need to use a high bandwidth differential or single ended probes (see Figure 17 on page 74). For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 392.

When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the 1134A probe amplifier.

When using a single differential probe head, use oscilloscope channel 2.

3 Connect adequate load to the power supply to assure it is regulating and turned on. Generally, one IDE hard drive will provide adequate load.

4 Turn on the power supply. DS1 LED (located near the ATX power supply connector) should turn on. If the LED is on, but the power supply does not turn on, check that the jumper J7 is installed between J7-1 and J7-2.

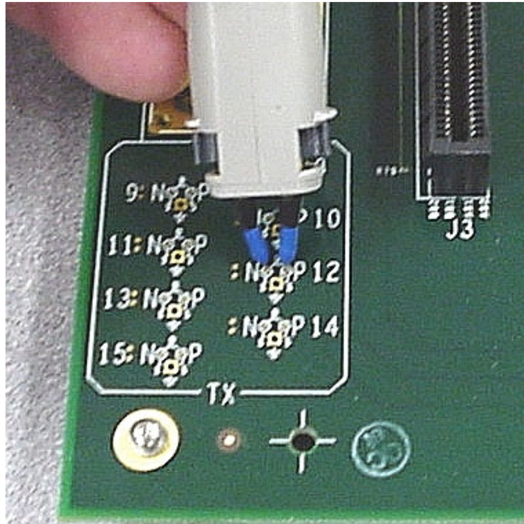


Figure 17 Compliance Base Board (CBB) Active Probing Option

Running Add-In Card Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 22. Then, when selecting tests, navigate to the "Add-In Card (Tx) Tests" group.

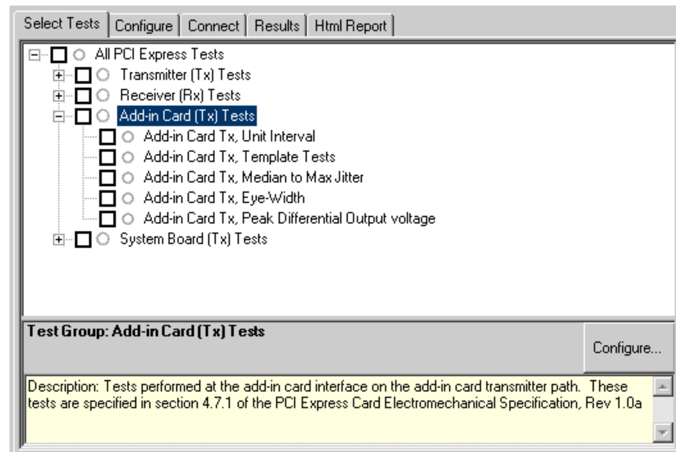


Figure 18 Selecting Add-In Card (Tx) Tests

Unit Interval

Table 36 UI from Table 4-5 of the Base Specification

Symbol	Parameter	Min	Nom	Max
UI	Unit Interval	399.88 ps	400ps	400.12 ps

Test Definition Notes from the Specification

- UI (Unit Interval) is specified to be +/-300 ppm.
- UI does not account for SSC dictated variations.
- UI is defined in Table 4-5 (Base Specification).
- UI Characteristics are Maximum UI =400.12 ps and Minimum UI = 399.88ps.

Test Procedure

Follow the procedure in "Running Add-In Card Tests" on page 75, and select "Unit Interval".

PASS Condition

399.88ps < UI < 400.12ps

Measurement Algorithm

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window.

TX UI(p) = Mean(UI(n))

Where:

n is the index of UI in the clock recovery window.

p indicates the pth 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI, as described below.

NOTE The UI measurement is not required at this point. It is provided as an informative test only.

NOTE The TX UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another TX UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case TX UI is reported.

Test References

Table 37 Unit Interval Test References

Test Name	Reference	PCI-SIG Assertions
Unit Interval	This test is not required. It is informative only.	

Template Tests

See Section 4.7.1 of the Card Electromechanical Specification for additional notes and test definitions.

Test Definition Notes from the Specification

Table 38 Table 4-6 of the Card Electromechanical Specification.

Parameter	Value	Notes
Vtx_A	>= 514 mV	All Links are assumed active while generating this eye diagram. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (Ttx_A_d).
Vtx_A_d	>= 360 mV	
Ttx_A	>= 237 ps	

- Note: The values in Table 38 are referenced to an ideal 100 ohm differential load at the end of the interconnect path at the edge-finger boundary on the add-in card. The eye diagram is defined and centered with respect to the jitter median. The jitter median should be calculated across any 250 consecutive UIs. The maximum jitter outlier should be no greater than 81.5 ps away from the jitter median.

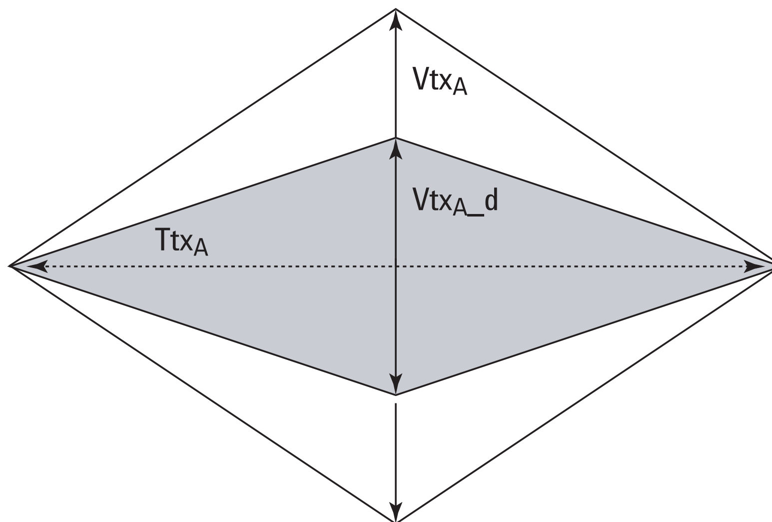


Figure 19 Add-In Card Tx Compliance Eye Diagram

Test References

Table 39 Template Tests Test References

Test Name	Reference	PCI-SIG Assertions
Template Tests	PCI Express CEM Specification, Rev 1.0a, Section 4.7.1, Figure 4-8	EM.4#19

Median to Max Jitter

Table 40 $Ttx_{A\text{-MEDIAN-to-MAX-JITTER}}$ for Add-In Card

Symbol	Parameter	Min	Nom	Max
$Ttx_{A\text{-MEDIAN-to-MAX-JITTER}}$	Maximum time between the jitter median and maximum deviation from the median.			81.5 ps

Test Definition Notes from the Specification

- Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to the recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used to calculate the TX UI.
- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured over any 250 consecutive TX UIs. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).
- A Ttx_A >= 237 ps provides for a total sum of deterministic and random jitter budget of $Ttx_{A-MAX-JITTER}$ = 163 ps for the Transmitter collected over any 250 consecutive TX UIs. The $Ttx_{A-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs.

  It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
- $Ttx_{A-MEDIAN-to-MAX-JITTER}$ (Maximum time between the jitter median and maximum deviation from the median.) is defined in Table 4-6 (Card Electromechanical Specification).

Limits

Maximum = 81.5 ps

Pass Condition

81.5 ps > $Ttx_{A-MEDIAN-to-MAX-JITTER}$

Test Procedure

Follow the procedure in “Running Add-In Card Tests" on page 75, and select “Median to Max Jitter”.

Measurement Algorithm

This measurement is made over 250 consecutive bits defined in Section 3.4 (Base Specification).

The measured time difference between a data edge and a recovered clock edge.

$$tie(n) = t_{R-DAT}(n) - t_{DAT}(n)$$

Where:

t_{DAT} is the original data edge.

t_{R-DAT} is the recovered data edge (the ideal time of the data edge as defined by the recovered clock around t_{DAT}).

n is the index of all edges in the waveform.

Test References

Table 41 Median to Max Jitter Test References

Test Name	Reference	PCI-SIG Assertions
Median to Max Jitter	PCI Express CEM Specification, Rev 1.0a, Table 4-6	EM.4#13, EM.4#19

Eye-Width

Table 42 Ttx_A for Add-In Card

Symbol	Parameter	Min	Nom	Max
Ttx_A	Minimum TX Eye Width	237 ps		

Test Definition Notes from the Specification

- The maximum Transmitter jitter can be derived as $Ttx_{A-MAX-JITTER}$ = 400 ps – Ttx_A = 163 ps.
- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured over any 250 consecutive TX UIs. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).
- A Ttx_A = 237 ps provides for a total sum of deterministic and random jitter budget of $Ttx_{A-MAX-JITTER}$ = 163 ps for the Transmitter collected over any 250 consecutive TX UIs. The $Ttx_{A-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs.

NOTE

The median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

- Ttx_A (Minimum TX Eye Width) is defined in Table 4-6 (Card Electromechanical Specification).

Limits

Minimum = 237 ps

Pass Condition

237 ps <= Ttx_A

Test Procedure

Follow the procedure in "Running Add-In Card Tests" on page 75, and select "Eye-Width".

Measurement Algorithm

This measurement is made over 250 consecutive bits defined in Section 3.4 (Base Specification).

The measured minimum horizontal eye opening at the zero reference level as shown in the eye diagram.

$$T_{EYE-WIDTH} = UI_{AVG} - TIE_{Pk-Pk}$$

Where:

UI_{AVG} is the average UI.

TIE_{Pk-Pk} is the Peak-Peak TIE.

Test References

Table 43 Eye-Width Test References

Test Name	Reference	PCI-SIG Assertions
Eye-Width	PCI Express CEM Specification, Rev 1.0a, Table 4-6	EM.4#13, EM.4#19

Peak Differential Output Voltage

Table 44 $V_{TX-DIFFp-p}$ for Add-in Card

Symbol	Parameter	Min	Nom	Max
$V_{TX-DIFFp-p}$	Differential Pk-Pk Output Voltage	0.36 V		1.2 V

Test Definition Notes from the Specification

- $V_{TX-DIFFp-p} = 2*|V_{TX-D+} - V_{TX-D-}|$
- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured over any 250 consecutive TX UIs. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).

Test Procedure

Follow the procedure in “Running Add-In Card Tests" on page 75, and select “Peak Differential Output Voltage”.

PASS Condition

$0.36 \text{ V} \leq V_{TX-DIFF-p-p} \leq 1.2\text{V}$

Measurement Algorithm

The Differential Peak Voltage measurement returns two times the larger of the Min or Max statistic if the differential voltage waveform.

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}), Min(V_{DIFF(i)}))$$

Where:

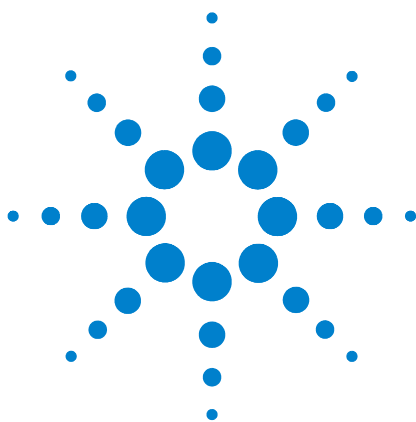
i is the index of all waveform values.

V_{DIFF} is the Differential Voltage signal.

Test References

Table 45 Peak Differential Output Voltage Test References

Test Name	Reference	PCI-SIG Assertions
Peak Differential Output Voltage	PCI Express Base Specification, Rev 1.0a, Table 4-6	EM.4#19



6
System Board (Tx) Tests, PCI-E 1.0a

Probing the Link for System Board Compliance 83
Running System Board Tests 85

This section provides the Methods of Implementation (MOIs) for System Board tests using an Agilent 54855A, 80000B, or 90000A Series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

Probing the Link for System Board Compliance

Connecting the Signal Quality Load Board for System/Motherboard Testing

There are multiple pairs of SMA connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1 With the system/motherboard powered off, connect the Compliance PCI Express Signal Quality Load Board into the connector under test. The PCI Express Signal Quality Load Board has edge fingers for x1, x4, x8 and x16 connectors.

   The PCI Express Signal Quality Load Board will cause a PCI Express 1.0a Base Specification System/motherboard to enter the compliance sub-state of the polling state. During this state the device under test will repeatedly send out the compliance pattern defined in the PCI Express Base Specification.

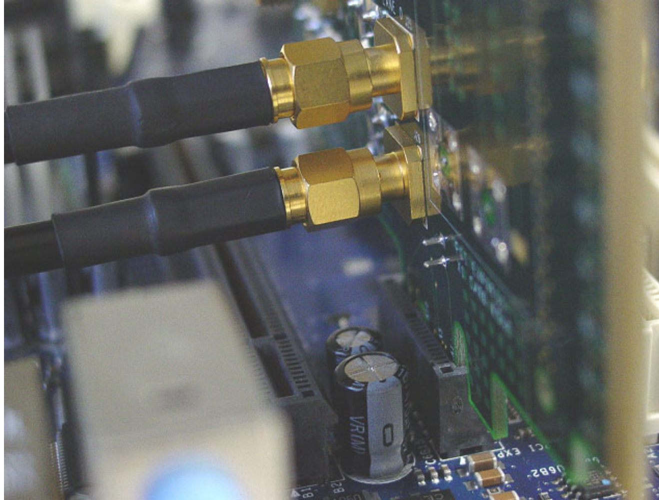


Figure 20 SMA Probing Option

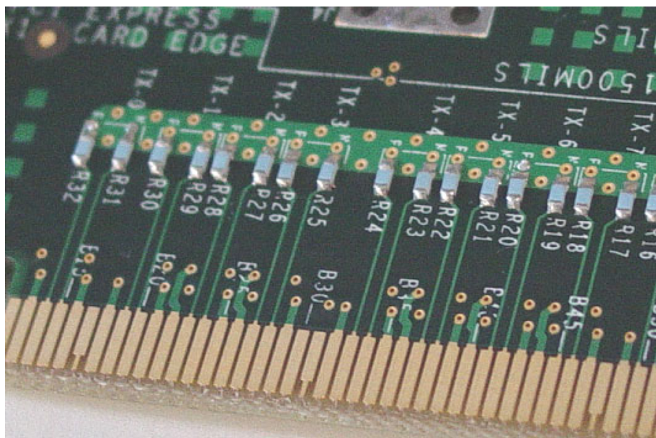


Figure 21 Resistor Terminations for Lanes without SMA Probing

2 Connect cables up as follows:

  a Digital Storage Oscilloscope channel 1 to TX LANE 1 P (where Lane 1 is under test).

  b Digital Storage Oscilloscope channel 3 to TX LANE 1 N (where Lane 1 is under test).

When SMA probing and two channels are used, channel-to-channel deskew is required (see “Channel-to-Channel De-skew" on page 386).

Not all lanes have SMA probing options. For signal quality testing of the remaining lanes you will need to use a high bandwidth differential or single ended probes (see Figure 17 on page 74). For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 392.

When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the 1134A probe amplifier.

When using a single differential probe head, use oscilloscope channel 2.

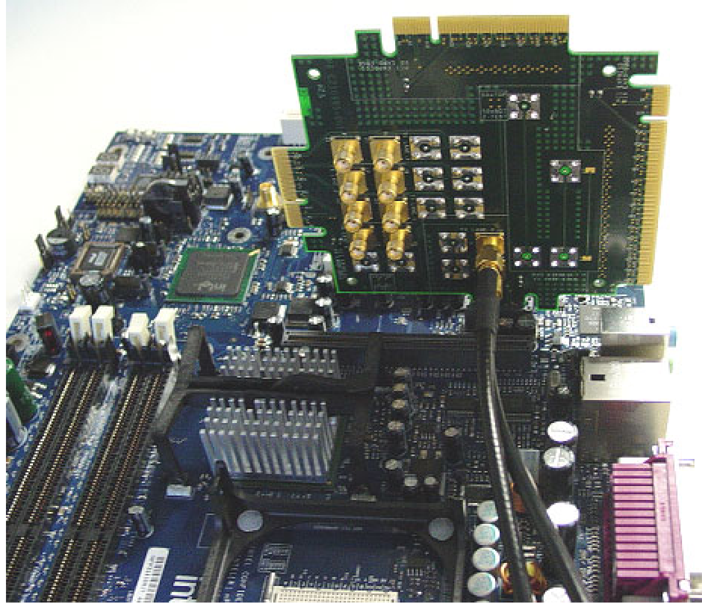


Figure 22 Connecting the PCI Express Signal Quality Test Fixture

Running System Board Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 22. Then, when selecting tests, navigate to the "System Board (Tx) Tests" group.

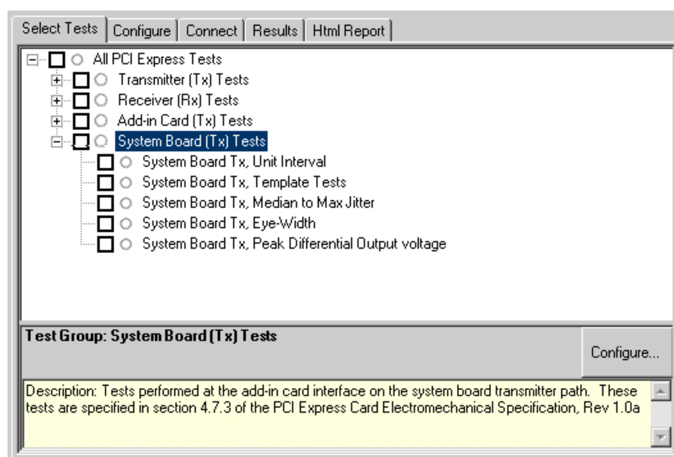


Figure 23 Selecting System Board (Tx) Tests

Unit Interval

Table 46 UI from Table 4-5 of the Base Specification

Symbol	Parameter	Min	Nom	Max
UI	Unit Interval	399.88 ps	400ps	400.12 ps

Test Definition Notes from the Specification

- UI (Unit Interval) is specified to be +/-300 ppm.
- UI does not account for SSC dictated variations.
- UI is defined in Table 4-5 (Base Specification).
- UI Characteristics are Maximum UI =400.12 ps and Minimum UI = 399.88ps.

Test Procedure

Follow the procedure in “Running System Board Tests" on page 85, and select “Unit Interval”.

PASS Condition

399.88ps < UI < 400.12ps

Measurement Algorithm

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window.

TX UI(p) = Mean(UI(n))

Where:

n is the index of UI in the clock recovery window.

p indicates the pth 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI, as described below.

NOTE The UI measurement is not required at this point. It is provided as an informative test only.

NOTE The TX UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another TX UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case TX UI is reported.

Test References

Table 47 Unit Interval Test References

Test Name	Reference	PCI-SIG Assertions
Unit Interval	This test is not required. It is informative only.	

Template Tests

See Section 4.7.3 of the Card Electromechanical Specification for additional notes and test definitions.

Test Definition Notes from the Specification

Table 48 Table 4-8 of the Card Electromechanical Specification

Parameter	Value	Notes
Vtx_S	>= 274 mV	All Links are assumed active while generating this eye diagram. Transition and nontransition bits must be distinguished in order to measure compliance against the deemphasized voltage level (Ttx_S_d).
Vtx_S_d	>= 253 mV	
Ttx_S	>= 183 ps	

- Note: The values in Table 48 are referenced to an ideal 100 ohm differential load at the end of the interconnect path at the isolated edge-finger boundary of an add-in card when mated with a connector. The eye diagram is defined and centered with respect to the jitter median. The jitter median should be calculated across any 250 consecutive UIs. The maximum jitter outlier should be no greater than 108.5 ps away from the jitter median.

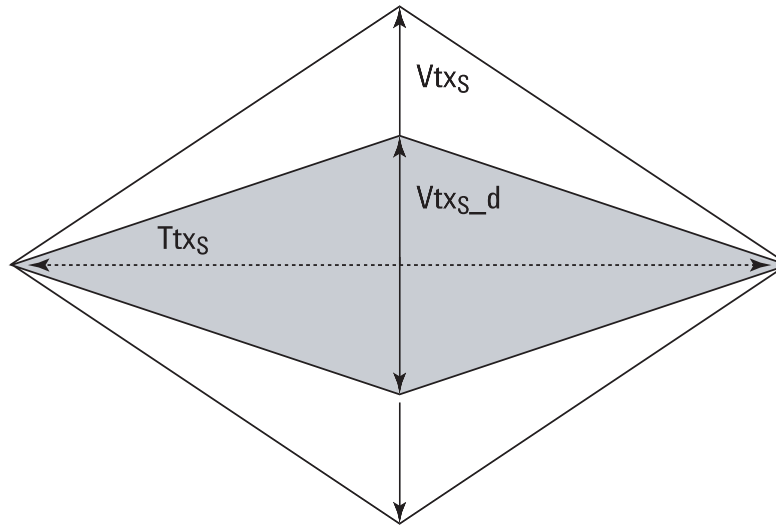


Figure 24 System Board Tx Compliance Eye Diagram

Test References

Table 49 Template Tests Test References

Test Name	Reference	PCI-SIG Assertions
Template Tests	PCI Express CEM Specification, Rev 1.0a, Section 4.7.3, Figure 4-10	EM.4#20, EM.4#14

Median to Max Jitter

Table 50 $Ttx_{S\text{-MEDIAN-to-MAX-JITTER}}$ for System Board

Symbol	Parameter	Min	Nom	Max
$Ttx_{S\text{-MEDIAN-to-MAX-JITTER}}$	Maximum time between the jitter median and maximum deviation from the median.			108.5 ps

Test Definition Notes from the Specification

- Jitter is defined as the measurement variation of the crossing points ($V_{TX\text{-}DIFFp\text{-}p}$ = 0 V) in relation to the recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used to calculate the TX UI.

- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured over any 250 consecutive TX UIs. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).
- A Ttx_{S} >= 183 ps provides for a total sum of deterministic and random jitter budget of $Ttx_{S-MAX-JITTER}$ = 217 ps for the Transmitter collected over any 250 consecutive TX UIs. The $Ttx_{S-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs.

  It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
- $Ttx_{S-MEDIAN-to-MAX-JITTER}$ (Maximum time between the jitter median and maximum deviation from the median) is derived from Table 4-8 (Card Electromechanical Specification).

Limits

Maximum = 108.5 ps

Pass Condition

108.5 ps > $Ttx_{S-MEDIAN-to-MAX-JITTER}$.

Test Procedure

Follow the procedure in “Running System Board Tests" on page 85, and select “Median to Max Jitter”.

Measurement Algorithm

This measurement is made over 250 consecutive bits defined in Section 3.4 (Base Specification).

The measured time difference between a data edge and a recovered clock edge.

$$tie(n) = t_{R-DAT}(n) - t_{DAT}(n)$$

Where:

t_{DAT} is the original data edge.

t_{R-DAT} is the recovered data edge (the ideal time of the data edge as defined by the recovered clock around t_{DAT}).

n is the index of all edges in the waveform.

Test References

Table 51 Median to Max Jitter Test References

Test Name	Reference	PCI-SIG Assertions
Median to Max Jitter	PCI Express CEM Specification, Rev 1.0a, Table 4-8	EM.4#20, EM.4#14

Eye-Width

Table 52 Ttx_S for System Board

Symbol	Parameter	Min	Nom	Max
Ttx_S	Minimum TX Eye Width	183 ps		

Test Definition Notes from the Specification

- The maximum Transmitter jitter can be derived as $Ttx_{S-MAX-JITTER}$ = 400 ps – Ttx_S = 217 ps.
- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured over any 250 consecutive TX UIs. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).
- A Ttx_S = 183 ps provides for a total sum of deterministic and random jitter budget of $Ttx_{S-MAX-JITTER}$ = 217 ps for the Transmitter collected over any 250 consecutive TX UIs. The $Ttx_{S-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs.

NOTE The median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

- Ttx_S (Minimum TX Eye Width) is defined in Table 4-8 (Card Electromechanical Specification).

Limits

Minimum = 183 ps

Pass Condition

183 ps <= Ttx_S.

Test Procedure

Follow the procedure in “Running System Board Tests" on page 85, and select “Eye-Width”.

Measurement Algorithm

This measurement is made over 250 consecutive bits defined in Section 3.4 (Base Specification).

The measured minimum horizontal eye opening at the zero reference level as shown in the eye diagram.

$$T_{EYE-WIDTH} = UI_{AVG} - TIE_{Pk-Pk}$$

Where:

UI_{AVG} is the average UI.

TIE_{Pk-Pk} is the Peak-Peak TIE.

Test References

Table 53 Eye-Width Test References

Test Name	Reference	PCI-SIG Assertions
Eye-Width	PCI Express CEM Specification, Rev 1.0a, Table 4-8	EM.4#20, EM.4#14

Peak Differential Output Voltage

Table 54 $V_{TX-DIFFp-p}$ for System Board

Symbol	Parameter	Min	Nom	Max
$V_{TX-DIFFp-p}$	Differential Pk-Pk Output Voltage	0.253 V		1.2 V

Test Definition Notes from the Specification

- $V_{TX-DIFFp-p} = 2*|V_{TX-D+} - V_{TX-D-}|$
- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured over any 250 consecutive TX UIs. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).

Test Procedure

Follow the procedure in “Running System Board Tests" on page 85, and select “Peak Differential Output Voltage”.

PASS Condition

0.253 V <= $V_{TX-DIFF-p-p}$ <= 1.2V

Measurement Algorithm

The Differential Peak Voltage measurement returns two times the larger of the Min or Max statistic if the differential voltage waveform.

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}), Min(V_{DIFF(i)}))$$

Where:

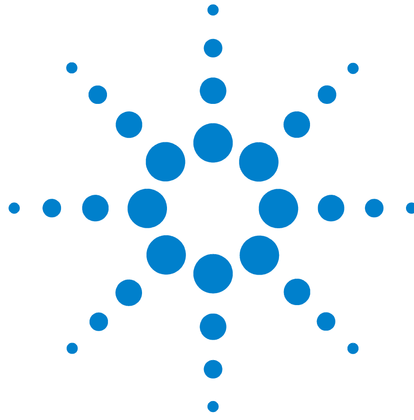
i is the index of all waveform values.

V_{DIFF} is the Differential Voltage signal.

Test References

Table 55 Peak Differential Output Voltage Test References

Test Name	Reference	PCI-SIG Assertions
Peak Differential Output Voltage	PCI Express CEM Specification, Rev 1.0a, Table 4-8	EM.4#20



Part III
PCI Express Version 1.1

Agilent Technologies

7
Reference Clock Tests, PCI-E 1.1

Probing the Link for Reference Clock Compliance 96
Reference Clock Measurement Point 100
Running Reference Clock Tests 100

This section provides the Methods of Implementation (MOIs) for Reference Clock tests using an Agilent 54855A, 80000B, or 90000A Series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

Probing the Link for Reference Clock Compliance

Reference Clock tests are done by connecting the device under test to a test fixture and probing the SMA connectors on the test fixture. To probe the reference clock link, you can:

- Use two 50-ohm coax cables with SMA male connectors, two precision 3.5 mm BNC to SMA male adapters (54855-67604, included with the oscilloscope), and the channel 1 and channel 3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.
- Use two differential probe heads with two 1134A probe amplifiers (with the negative lead grounded for single-ended measurements) and the channel 1 and channel 3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.
- Use one differential probe head with the 1134A probe amplifier and the channel 2 input of an oscilloscope that has 20 GS/s sample rate available on that channel.

When the link is broken and terminated into a 50 ohm load (by the test load), the Compliance Pattern defined in section 4.2.8 (Card Electromechanical Specification) will be transmitted.

Table 56 Probing Options for Reference Clock Testing

	Probing Configurations			Captured Waveforms		Oscilloscope Specifications	
	Probing Method	**Break Serial Link**	**Channels Used**	**Differential Mode**	**Common Mode**	**System Band Width**	**Rise* Time (20-80)**
DUT Connection	Single-Ended SMA (2 x 50-Ohm SMA Cables)	Y	2	Pseudo	Yes	6 GHz	70 ps
	Single-Ended (2 x 1134A w/ Differential Probe Heads)	Y/N	2	Pseudo	Yes	6 GHz	70 ps
	Differential (1 x 1134A w/ Differential Probe Head)	Y/N	1	True	No	6 GHz	70 ps

*Typical

Single-Ended SMA Probing

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Source 1-Source 2. The Sources can be either channels 1 and 3 or channels 2 and 4. The Common mode measurements are also available in this configuration from the common mode waveform (Source 1 + Source 2)/2.

This probing technique requires breaking the link and terminating into the 50 ohm/side termination into the oscilloscope. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Channel-to-Channel deskew is required using this technique because two channels are used.

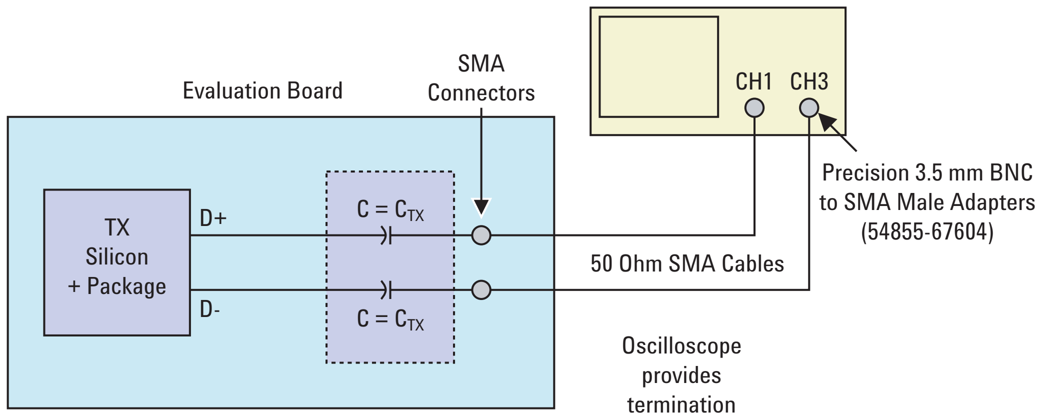


Figure 25 Single-Ended SMA Probing using Channel 1 and Channel 3

Single-Ended Probing

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Source 1 - Source 2. The Sources can be either channels 1 and 3 or channels 2 and 4. The Common mode measurements are also available in this configuration from the common mode waveform (Source 1 + Source 2)/2.

Make sure to probe equal distances from the reference clock, as close as possible to the reference clock. Place single-ended grounds as close to the signal line's reference ground as possible. Channel-to-Channel deskew is required using this probing technique because two channels are used.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, "InfiniiMax Probing Options," starting on page 392.

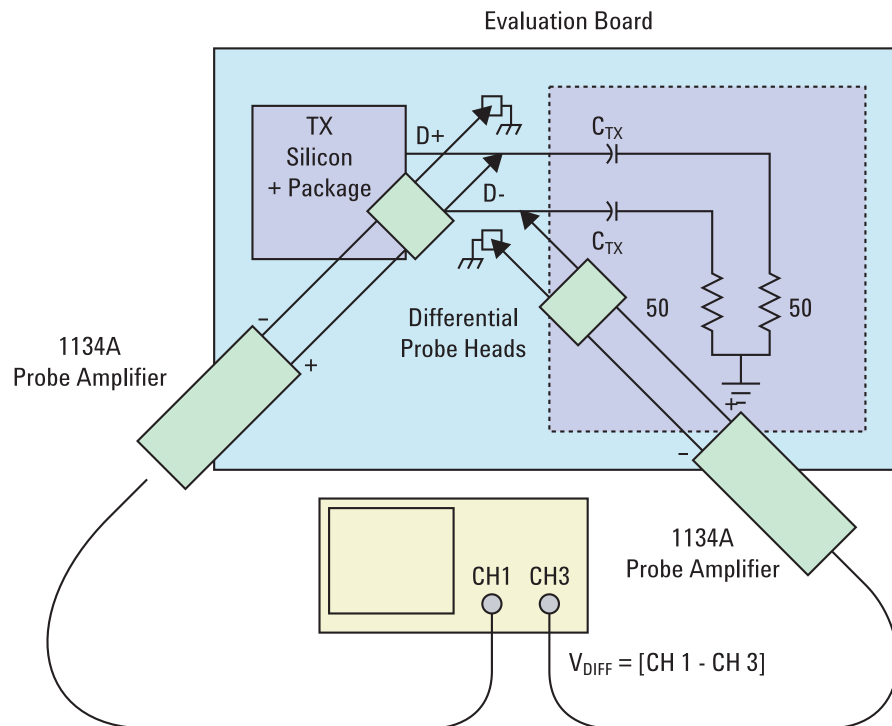


Figure 26 Single-Ended Probing

Differential Probing

The differential signal is measured directly by the differential probe head.

Make sure to probe equal distances from the reference clock, as close as possible to the reference clock.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Only one channel of the oscilloscope is used.

For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 392.

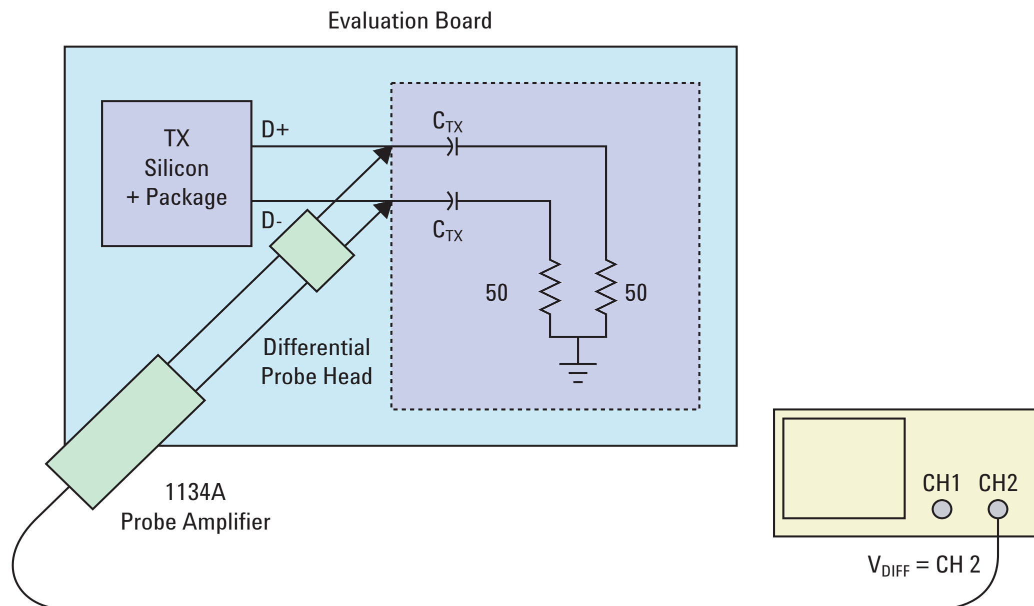


Figure 27 Differential Probing

Reference Clock Measurement Point

The compliance test load for driver compliance is shown in Figure 4-25 of the Card Electromechanical Specification.

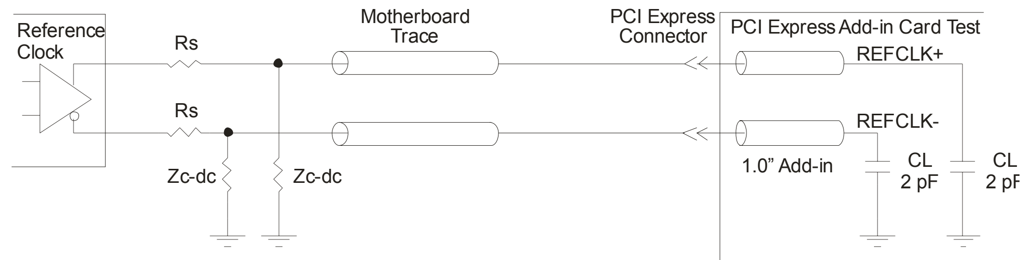


Figure 28 Driver Compliance Test Load.

Running Reference Clock Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 22. Then, when selecting tests, navigate to the "Reference Clock Tests" group.

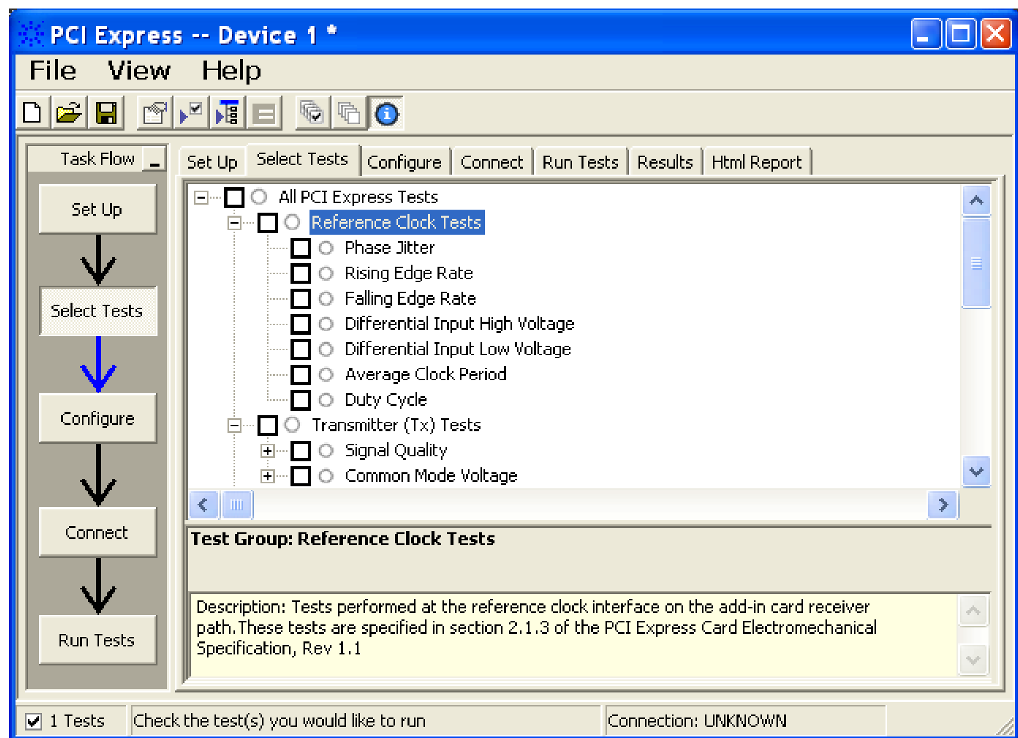


Figure 29 Selecting Reference Clock Tests

Phase Jitter

See Section 2.1.4 of the Card Electromechanical Specification Rev. 1.1 for additional notes and test definitions.

Table 57 Phase Jitter from Table 2-2 of the Card Electromechanical Specification Rev. 1.1.

Symbol	Parameter	Max
Phase Jitter	Phase Jitter (BER 10^{-6})	86 ps

Test Procedure

Follow the procedure in "Running Reference Clock Tests" on page 100, and select "Phase Jitter".

Note that you can use the "Stitch Method" configuration setting to select the method used to stitch the waveform for the reference clock phase jitter test:

- Absolute — this method stitches the waveform based on absolute data.
- Dynamic — this method aligns waveform data to have common offset before stitching.

This "Stitch Method" configuration setting only applies when Spread Sprectrum Clocking is enabled.

Pass Condition

≤ 86 ps

Test Definition Notes from the Specification

- Measurement taken from differential waveform using the circuit shown in Figure 28 on page 100.

Measurement Algorithm

Phase jitter is measured using the clock time interval error measurement with a bit error rate of 10^{-6}.

Test References

Table 58 Phase Jitter Test References

Test Name	Reference	PCI-SIG Assertions
Phase Jitter	PCI Express Card Electromechanical Specification, Rev 1.1, Table 2-2	PHY.3.3#2

Rising Edge Rate

See Section 2.1.3 of the Card Electromechanical Specification for additional notes and test definitions.

Table 59 Rise Edge Rate from Table 2-1 of the Card Electromechanical Specification Rev. 1.1.

Symbol	Parameter	Min	Max
Rise Edge Rate	Rising Edge Rate	0.6 V/ns	4.0 V/ns

Test Procedure

Follow the procedure in “Running Reference Clock Tests" on page 100, and select “Rising Edge Rate”.

Pass Condition

0.6 V/ns ≥ Rising Edge Rate ≤ 4.0 V/ns

Test Definition Notes from the Specification

- Measurement taken from differential waveform using the circuit shown in Figure 28 on page 100.
- Measurement taken from differential waveform.
- Measured from the -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-).The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement widow is centered on the differential zero crossing. See Figure 30 on page 103

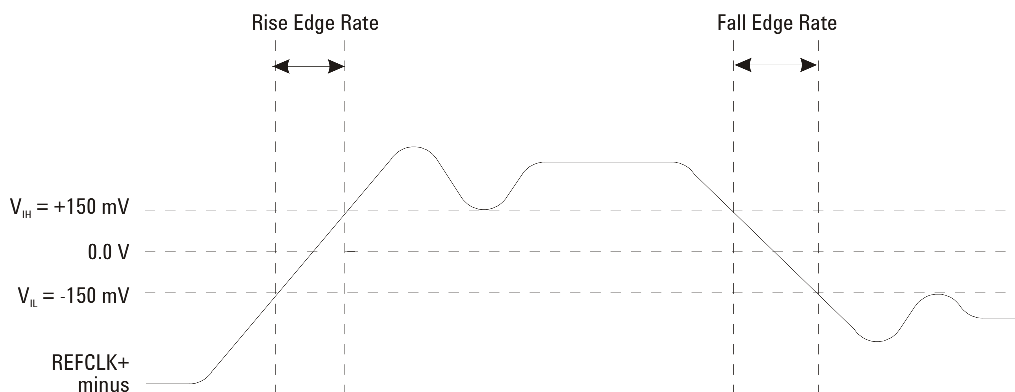


Figure 30 Differential Measurement Points for Rise Edge and Fall Edge Rate.

Test References

Table 60 Rising Edge Rate References

Test Name	Reference	PCI-SIG Assertions
Rising Edge Rate	PCI Express Card Electromechanical Specification, Rev 1.1, Section 2.1.3 Table 2-1	PHY.3.3#1

Falling Edge Rate

See Section 2.1.3 of the Card Electromechanical Specification for additional notes and test definitions.

Table 61 Falling Edge Rate from Table 2-1 of the Card Electromechanical Specification Rev. 1.1.

Symbol	Parameter	Min	Max
Fall Edge Rate	Falling Edge Rate	0.6 V/ns	4.0 V/ns

Test Procedure

Follow the procedure in "Running Reference Clock Tests" on page 100, and select "Falling Edge Rate".

Pass Condition

0.6 V/ns ≤ Falling Edge Rate ≤ 4.0 V/ns

Test Definition Notes from the Specification

- Measurement taken from differential waveform using the circuit shown in Figure 28 on page 100.
- Measurement taken from differential waveform.
- Measured from the -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-).The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement widow is centered on the differential zero crossing. See Figure 30 on page 103

Test References

Table 62 Falling Edge Rate References

Test Name	Reference	PCI-SIG Assertions
Falling Edge Rate	PCI Express Card Electromechanical Specification, Rev 1.1, Section 2.1.3 Table 2-1	PHY.3.3#1

Differential Input High Voltage

See Section 2.1.3 of the Card Electromechanical Specification for additional notes and test definitions.

Table 63 V_{IH} from Table 2-1 of the Card Electromechanical Specification.

Symbol	Parameter	Min
V_{IH}	Differential input high voltage	150 mV

Test Procedure

Follow the procedure in “Running Reference Clock Tests" on page 100, and select “Differential Input High Voltage”.

Pass Condition

$V_{IH} > 150$ mV

Test Definition Notes from the Specification

- Measurement taken from differential waveform using the circuit shown in Figure 28 on page 100.

Measurement Algorithm

Figure 30 on page 103 shows the measurement point for the differential input high voltage measurement.

Test References

Table 64 Differential Input High Voltage

Test Name	Reference	PCI-SIG Assertions
Differential Input High Voltage	PCI Express Card Electromechanical Specification, Rev 1.1, Table 2-1	PHY.3.3#4

Differential Input Low Voltage

Table 65 V_{IH} from Table 2-1 of the Card Electromechanical Specification.

Symbol	Parameter	Max
V_{IL}	Differential input low voltage	-150 mV

Test Procedure

Follow the procedure in "Running Reference Clock Tests" on page 100, and select "Differential Input Low Voltage".

Pass Condition

$V_{IL} < -150$ mV

Test Definition Notes from the Specification

- Measurement taken from differential waveform using the circuit shown in Figure 28 on page 100.

Measurement Algorithm

Figure 30 on page 103 shows the measurement point for the differential input low voltage measurement.

Test References

Table 66 Differential Input Low Voltage

Test Name	Reference	PCI-SIG Assertions
Differential Input Low Voltage	PCI Express Card Electromechanical Specification, Rev 1.1, Table 2-1	PHY.3.3#4

Average Clock Period

Table 67 $T_{PERIOD\ AVG}$ from Table 2-1 of the Card Electromechanical Specification.

Symbol	Parameter	Min	Max
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	-300 ppm	2800 ppm

Test Procedure

Follow the procedure in "Running Reference Clock Tests" on page 100, and select "Average Clock Period".

Pass Condition

$-300\ ppm \leq V_{PERIOD\ AVG} \leq 2800\ ppm$

Test Definition Notes from the Specification

- Measurement taken from differential waveform using the circuit shown in Figure 28 on page 100.
- PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is $1/1{,}000{,}000^{th}$ of 100.000000 MHz exactly or 100 Hz. For 300 PPM there is an error budget of 100 Hz/PPM * 300 PPM = 30 kHz. The period is to be measured with a frequency counter with measurement window set to 100 ms or greater. The 300 PPM applies to systems that do not employ Spread Spectrum or that use a common clock source. For systems employing Spread Spectrum there is an additional 2500 PPM nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of 2800 PPM.

Measurement Algorithm

Figure 31 on page 109 shows the measurement points for the period measurement.

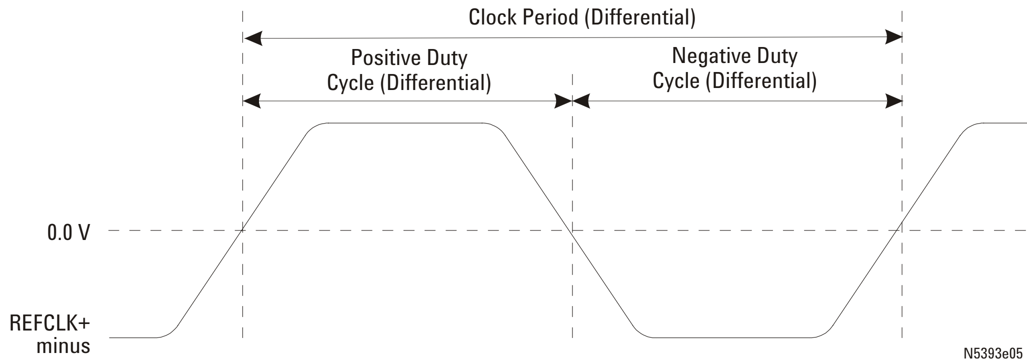


Figure 31 Differential Measurement Points for Clock Period and Duty Cycle.

Test References

Table 68 Average Clock Period

Test Name	Reference	PCI-SIG Assertions
Average Clock Period	PCI Express Card Electromechanical Specification, Rev 1.1, Table 2-1	PHY.3.3#9

Duty Cycle

Table 69 $V_{REFERENCE\ CLOCK\text{-}DIFFp\text{-}p}$ from Table 4-5 of the Card Electromechanical Specification.

Symbol	Parameter	Min	Max
Duty Cycle	Duty Cycle	40%	60%

Test Procedure

Follow the procedure in "Running Reference Clock Tests" on page 100, and select "Duty Cycle".

Pass Condition

40% ≤ Duty Cycle ≤ 60%

Test Definition Notes from the Specification

- Measurement taken from differential waveform using the circuit shown in Figure 28 on page 100.

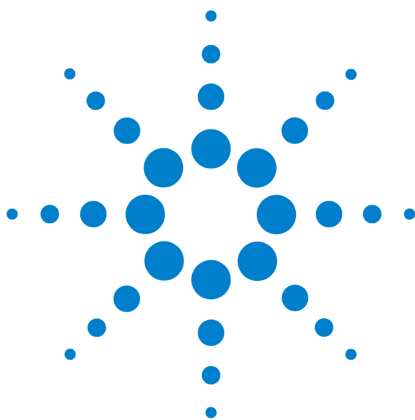
Measurement Algorithm

Figure 31 on page 109 shows the measurement points for the duty cycle measurement.

Test References

Table 70 Duty Cycle

Test Name	Reference	PCI-SIG Assertions
Duty Cycle	PCI Express Card Electromechanical Specification, Rev 1.1, Table 2-1	PHY.3.2#2



8
Transmitter (Tx) Tests, PCI-E 1.1, Full Power

Probing the Link for Tx Compliance 112
Tx Compliance Test Load 116
Running Signal Quality Tests 116
Running Common Mode Voltage Tests 129

This section provides the Methods of Implementation (MOIs) for Transmitter tests using an Agilent 54855A, 80000B, or 90000A series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

Probing the Link for Tx Compliance

Transmitter tests are done by connecting the device under test to a test fixture and probing the SMA connectors on the test fixture. To probe the transmitter link, you can:

- Use two 50-ohm coax cables with SMA male connectors, two precision 3.5 mm BNC to SMA male adapters (54855-67604, included with the oscilloscope), and the channel 1 and channel 3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.
- Use two differential probe heads with two 1134A probe amplifiers (with the negative lead grounded for single-ended measurements) and the channel 1 and channel 3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.
- Use one differential probe head with the 1134A probe amplifier and the channel 2 input of an oscilloscope that has 20 GS/s sample rate available on that channel.

When the link is broken and terminated into a 50 ohm load (by the test load), the Compliance Pattern defined in section 4.2.8 (Base Specification) will be transmitted.

Table 71 Probing Options for Transmitter Testing

	Probing Configurations			Captured Waveforms		Oscilloscope Specifications	
	Probing Method	**Break Serial Link**	**Channels Used**	**Differential Mode**	**Common Mode**	**System Band Width**	**Rise* Time (20-80)**
DUT Connection	Single-Ended SMA (2 x 50-Ohm SMA Cables)	Y	2	Pseudo	Yes	6 GHz	70 ps
	Single-Ended (2 x 1134A w/ Differential Probe Heads)	Y/N	2	Pseudo	Yes	6 GHz	70 ps
	Differential (1 x 1134A w/ Differential Probe Head)	Y/N	1	True	No	6 GHz	70 ps

*Typical

Single-Ended SMA Probing

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Source 1 - Source 2. The Sources can be either channels 1 and 3 or channels 2 and 4. The Common mode measurements are also available in this configuration from the common mode waveform (Source 1 + Source 2)/2.

This probing technique requires breaking the link and terminating into the 50 ohm/side termination into the oscilloscope. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Channel-to-Channel deskew is required using this technique because two channels are used.

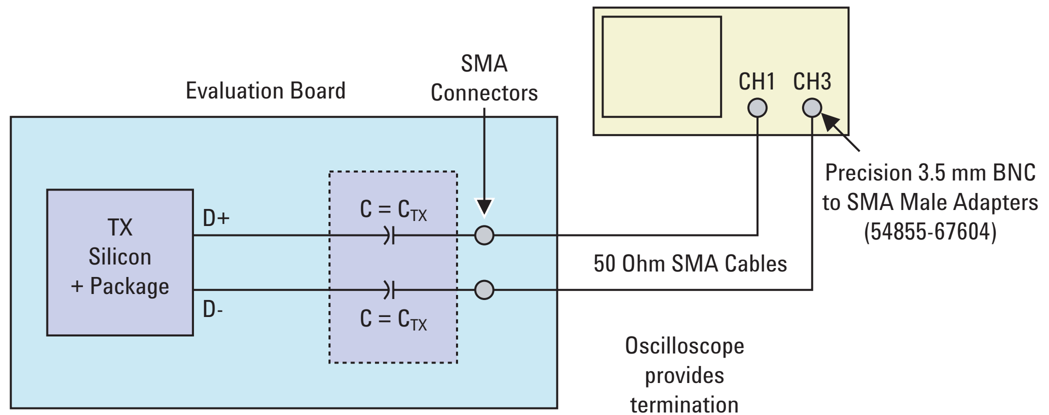


Figure 32 Single-Ended SMA Probing

Single-Ended Probing

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Source 1 - Source 2. The Sources can be either channels 1 and 3 or channels 2 and 4. The Common mode measurements are also available in this configuration from the common mode waveform (Source 1 + Source 2)/2.

Make sure to probe equal distances from the transmitter, as close as possible to the transmitter.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Channel-to-Channel deskew is required using this technique because two channels are used.

For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 392.

Place single-ended grounds as close to the signal line’s reference ground as possible.

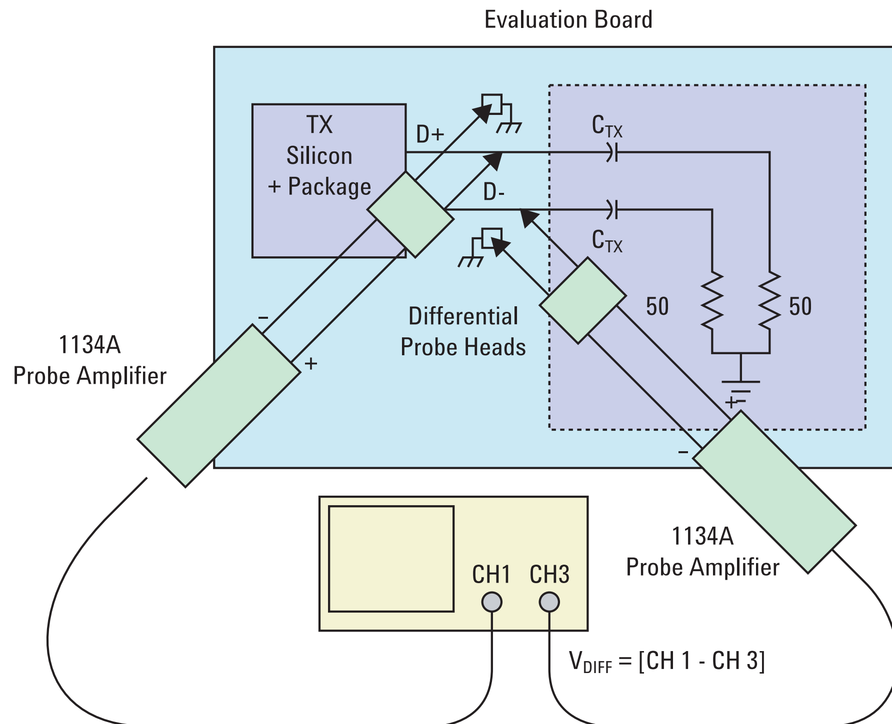


Figure 33 Single-Ended Probing

Differential Probing

The differential signal is measured directly by the differential probe head.

Make sure to probe equal distances from the transmitter, as close as possible to the transmitter.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Only one channel of the oscilloscope is used.

For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 392.

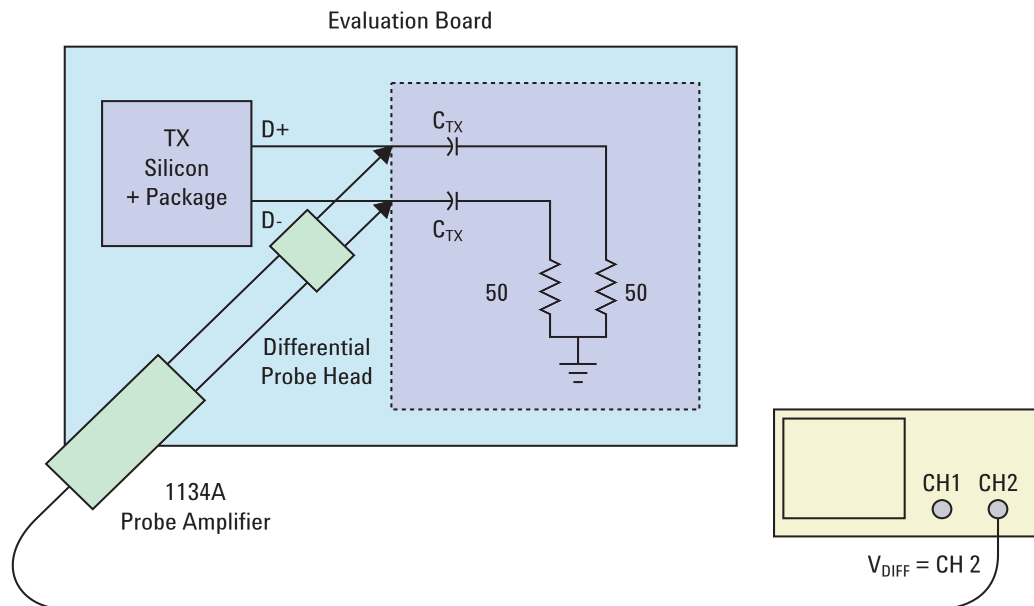


Figure 34 Differential Probing

Tx Compliance Test Load

The compliance test load for driver compliance is shown in Figure 4-25 (Base Specification)

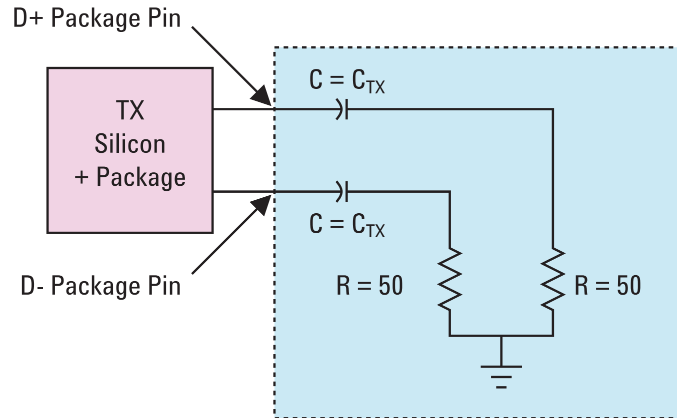


Figure 35 Driver Compliance Test Load.

Running Signal Quality Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 22. Then, when selecting tests, navigate to "Signal Quality" in the "Transmitter (Tx) Tests" group.

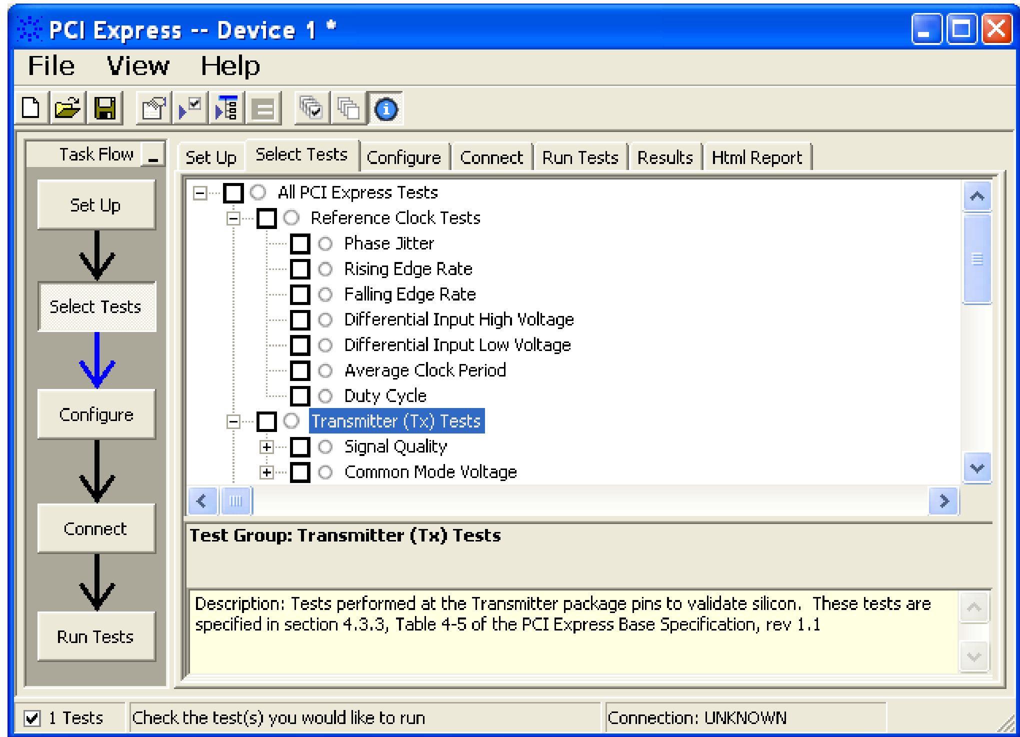


Figure 36 Selecting Transmitter (Tx) Signal Quality Tests

Unit Interval

Table 72 UI from Table 4-5 of the Base Specification.

Symbol	Parameter	Min	Nom	Max
UI	Unit Interval	399.88 ps	400ps	400.12 ps

Test Definition Notes from the Specification

- UI (Unit Interval) is specified to be ±300 ppm.
- UI does not account for SSC dictated variations.

Test Procedure

Follow the procedure in "Running Signal Quality Tests" on page 116, and select "Unit Interval".

Pass Condition

399.88ps < UI < 400.12ps

Measurement Algorithm

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window.

TX UI(p) = Mean(UI(n))

Where:

n is the index of UI in the current 3500 UI clock recovery window.

p indicates the pth 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI, as described below.

NOTE The TX UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another TX UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case TX UI is reported.

Test References

Table 73 Unit Interval Test References

Test Name	Reference	PCI-SIG Assertions
Unit Interval	PCI Express Base Specification, Rev 1.1, Table 4-5	PHY.3.3#2

Template Tests

See Section 4.3.3.1 of the Base Specification for additional notes and test definitions.

Test Definition Notes from the Specification

- The TX eye diagram in Figure 4-24 of the Base Specification is specified using the passive compliance/test measurement load in place of any real PCI Express interconnect + RX component.
- There are two eye diagrams that must be met for the Transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.
- The eye diagram must be valid for any 250 consecutive UIs.
- A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

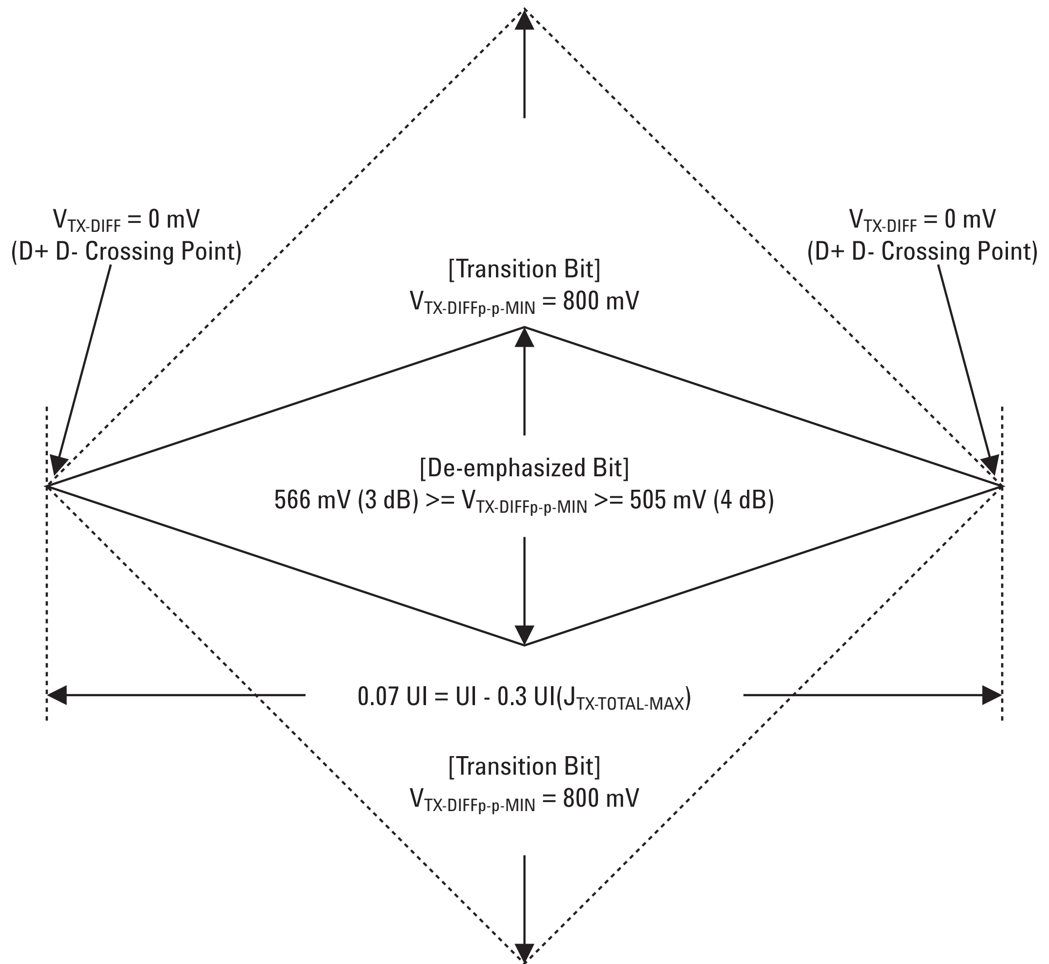


Figure 37 Minimum Transmitter Timing and Voltage Output Compliance Specification.

Test References

Table 74 Template Tests Test References

Test Name	Reference	PCI-SIG Assertions
Template Tests	PCI Express Base Specification, Rev 1.1, Section 4.3.3.1, Figure 4-26	PHY.3.3#1

Median to Max Jitter

Table 75 $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ from Table 4-5 of the Base Specification.

Symbol	Parameter	Min	Nom	Max
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.			0.125 UI

Test Definition Notes from the Specification

- Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to the recovered TX UI.
- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured using the clock recovery function specified in Section 4.3.3.2. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).

Limits

Maximum = 0.125 UI

Pass Condition

0.125 UI > $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$

Test Procedure

Follow the procedure in "Running Signal Quality Tests" on page 116, and select "Median to Max Jitter".

Measurement Algorithm

A T_{TX-EYE} = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.25 UI for the Transmitter using the clock recovery function specified in Section 4.3.3.2 of the Base Specification. $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget using the clock recovery function specified in Section 4.3.3.2 of the Base Specification.

It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. This parameter is measured with the equivalent of a zero jitter reference

clock. The T_{TX-EYE} measurement is to be met at the target bit error rate. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ is to be met using the compliance pattern at a sample size of 1,000,000 UI.

Test References

Table 76 Median to Max Jitter Test References

Test Name	Reference	PCI-SIG Assertions
Median to Max Jitter	PCI Express Base Specification, Rev 1.1, Table 4-5	PHY.3.3#4

Eye-Width

Table 77 T_{TX-EYE} from Table 4-5 of the Base Specification.

Symbol	Parameter	Min	Nom	Max
T_{TX-EYE}	Minimum TX Eye Width	0.75 UI		

Test Definition Notes from the Specification

- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured using the clock recovery function specified in Section 4.3.3.2. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).
- A T_{TX-EYE} = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.25 UI for the Transmitter using the clock recovery function specified in Section 4.3.3.2. $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget using the clock recovery function specified in Section 4.3.3.2.

  It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. This parameter is measured with the equivalent of a zero jitter reference clock. The T_{TX-EYE} measurement is to be met at the target bit error rate. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ is to be met using the compliance pattern at a sample size of 1,000,000 UI.

Limits

Minimum = 0.75 UI

Pass Condition

$0.75 \text{ UI} < T_{TX-EYE}$.

Test Procedure

Follow the procedure in "Running Signal Quality Tests" on page 116, and select "Eye-Width".

Measurement Algorithm

The maximum Transmitter jitter can be derived as follows.

$$T_{\text{TX-MAX-JITTER}} = 1 - T_{\text{TX-EYE}} = 0.25 \text{ UI}$$

This parameter is measured with the equivalent of a zero jitter reference clock.

Test References

Table 78 Eye-Width Test References

Test Name	Reference	PCI-SIG Assertions
Eye-Width	PCI Express Base Specification, Rev 1.1, Table 4-5	PHY.3.3#9

Peak Differential Output Voltage

Table 79 $V_{TX\text{-}DIFFp\text{-}p}$ from Table 4-5 of the Base Specification.

Symbol	Parameter	Min	Nom	Max
$V_{TX\text{-}DIFFp\text{-}p}$	Differential Pk-Pk Output Voltage	0.8 V		1.2 V

Test Definition Notes from the Specification

- This is the ration of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition.
- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured using the clock recovery function specified in Section 4.3.3.2. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).

Test Procedure

Follow the procedure in “Running Signal Quality Tests" on page 116, and select “Peak Differential Output Voltage”.

Pass Condition

$0.8\ V \leq V_{TX\text{-}DIFF\text{-}p\text{-}p} \leq 1.2\ V$

Measurement Algorithm.

$$V_{\text{TX-DIFFp-p}} = 2 \times |V_{\text{TX-D+}} - V_{\text{TX-DIFF-}}|$$

Test References

Table 80 Peak Differential Output Voltage Test References

Test Name	Reference	PCI-SIG Assertions
Peak Differential Output Voltage	PCI Express Base Specification, Rev 1.1, Table 4-5	PHY.3.2#2

Rise/Fall Time

Table 81 $T_{TX\text{-}RISE}$, $T_{TX\text{-}FALL}$ from Table 4-5 of the Base Specification.

Symbol	Parameter	Min	Nom	Max
$T_{TX\text{-}RISE}$, $T_{TX\text{-}FALL}$	D+/D- TX Output Rise/Fall Time	0.125 UI		

Test Definition Notes from the Specification

- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 of the Base Specification and measured using the clock recovery function specified in Section 4.3.3.2. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 of the Base Specification.
- Measured between 20-80% at Transmitter package pins into a test load as shown in Figure 4-25 for both $V_{TX\text{-}D+}$ and $V_{TX\text{-}D-}$.

Limits

Minimum = 0.125 UI

Pass Condition

0.125 UI < $T_{TX\text{-}RISE}$, $T_{TX\text{-}FALL}$.

Test Procedure

Follow the procedure in “Running Signal Quality Tests" on page 116, and select “Rise/Fall Time”.

Measurement Algorithms

Rise/Fall time is limited to only rising or falling edges of consecutive transitions for transmitter measurements. Rise/Fall Time is taken independently on each single ended waveform source when you use two single ended probes or two SMA cables as the signal source. Differential signal Rise/Fall Time show up when you select Differential probe type.

Rise Time. The Rise Time measurement is the time difference between when the VREF-HI reference level is crossed and the VREF-LO reference level is crossed on the rising edge of the waveform.

$$t_{RISE}(n) = t_{HI+}(i) - t_{LO+}(j)$$

Where:

t_{RISE} is a Rise Time measurement.

t_{HI+} is a set of t_{HI} for rising edges only.

t_{LO+} is a set of t_{LO} for rising edges only.

i and j are indexes for nearest adjacent pairs of t_{LO+} and t_{HI+}.

n is the index of rising edges in the waveform.

Rise Time for $v_{D+}(t)$ is as follows:

$t_{D+RISE}(n) = t_{D+HI+}(i) - t_{D+LO+}(j)$

and for $v_{D-}(t)$:

$t_{D-FALL}(n) = t_{D-LO-}(i) - t_{D-HI-}(j)$

Fall Time. The Fall Time measurement is the time difference between when the VREF-HI reference level is crossed and the VREF-LO reference level is crossed on the falling edge of the waveform.

$t_{FALL}(n) = t_{LO-}(i) - t_{HI-}(j)$

Where:

t_{FALL} is a Fall Time measurement.

t_{HI-} is set of t_{HI} for falling edge only.

t_{LO-} is set of t_{LO} for falling edge only.

i and j are indexes for nearest adjacent pairs of t_{LO-} and t_{HI-}.

n is the index of falling edges in the waveform.

Fall Time for $v_{D+}(t)$ is as follows:

$t_{D+FALL}(n) = t_{D+LO-}(i) - t_{D+HI-}(j)$

and for $v_{D-}(t)$:

$t_{D-FALL}(n) = t_{D-LO-}(i) - t_{D-HI-}(j)$

Test References

Table 82 Rise/Fall Time Test References

Test Name	Reference	PCI-SIG Assertions
Rise/Fall Time	PCI Express Base Specification, Rev 1.1, Table 4-5	PHY.3.3#3

De-emphasized Voltage Ratio

Table 83 $V_{TX-DE-RATIO}$ from Table 4-5 of the Base Specification.

Symbol	Parameter	Min	Nom	Max
$V_{TX-DE-RATIO}$	De-Emphasized Differential Output Voltage (Ratio)	-3.0 dB	-3.5 dB	-4.0 dB

Test Definition Notes from the Specification

- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 of the Base Specification and measured using the clock recovery function specified in Section 4.3.3.2 of the Base Specification. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 of the Base Specification.

Limits

Minimum = -3.0 dB and Maximum = -4.0 dB

Pass Condition

-4.0 dB < $V_{TX-DE-RATIO}$ < -3.0 dB.

Test Procedure

Follow the procedure in “Running Signal Quality Tests" on page 116, and select “De-emphasized Voltage Ratio”.

Measurement Algorithm

This is the ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.

Test References

Table 84 De-emphasized Voltage Ratio Test References

Test Name	Reference	PCI-SIG Assertions
De-emphasized Voltage Ratio	PCI Express Base Specification, Rev 1.1, Table 4-5	PHY.3.2#1

Running Common Mode Voltage Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 22. Then, when selecting tests, navigate to "Common Mode Voltage" in the "Transmitter (Tx) Tests" group.

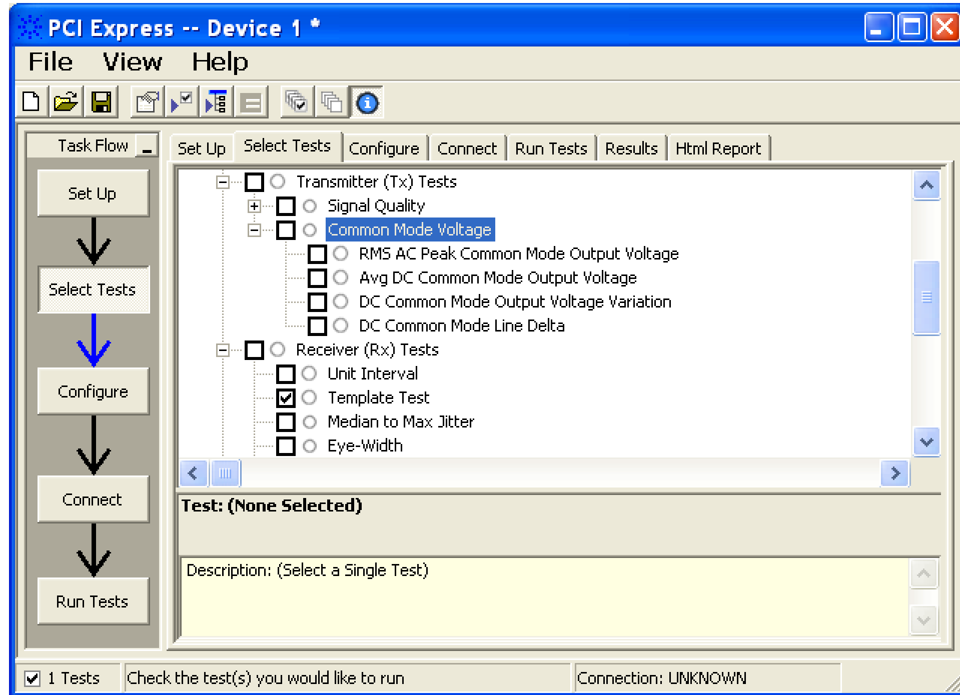


Figure 38 Selecting Transmitter (Tx) Common Mode Voltage Tests

RMS AC Peak Common Mode Output Voltage

Table 85 $V_{TX-CM-ACp}$ from Table 4-5 of the Base Specification.

Symbol	Parameter	Min	Nom	Max
$V_{TX-CM-ACp}$	RMS AC Peak Common Mode Output Voltage			20 mV

Test Definition Notes from the Specification

- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 of the Base Specification and measured using the clock recovery function specified in Section 4.3.3.2. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 of the Base Specification.

Limits

Maximum = 20 mV

Pass Condition

20 mV > $V_{TX-CM-ACp}$.

Test Procedure

Follow the procedure in “Running Common Mode Voltage Tests" on page 129, and select “RMS AC Peak Common Mode Output Voltage”.

NOTE This test is only available when the single-ended or SMA probing method has been used (see “Probing the Link for Tx Compliance" on page 112).

Measurement Algorithm

$$V_{\text{TX-CM-ACp}} = RMS\left(\frac{|V_{\text{TX-D+}} + V_{\text{TX-D-}}|}{2} - V_{\text{TX-CM-DC}}\right)$$

$$V_{\text{TX-CM-DC}} = DC_{(avg)} \text{ of } \frac{|V_{\text{TX-D+}} + V_{\text{TX-DC-}}|}{2}$$

Test References

Table 86 RMS AC Peak Common Mode Output Voltage Test References

Test Name	Reference	PCI-SIG Assertions
RMS AC Peak Common Mode Output Voltage	PCI Express Base Specification, Rev 1.1, Table 4-5	PHY.3.3#5

Avg DC Common Mode Output Voltage

Table 87 $V_{TX-DC-CM}$ from Table 4-5 of the Base Specification.

Symbol	Parameter	Min	Nom	Max
$V_{TX-DC-CM}$	The TX DC Common Mode Voltage	0 V		3.6 V

Test Definition Notes from the Specification

The allowed DC Common Mode voltage under any conditions. See Section 4.3.1.8 of the Base Specification.

- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured using the clock recovery function specified in Section 4.3.3.2. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).

Limits

$0\ V \le V_{TX-DC-CM} \le 3.6\ V$

Test Procedure

Follow the procedure in “Running Common Mode Voltage Tests" on page 129, and select “Avg DC Common Mode Output Voltage”.

NOTE This test is only available when the single-ended or SMA probing method has been used (see “Probing the Link for Tx Compliance" on page 112).

Measurement Algorithm

The Avg DC Common Mode Voltage measurement computes the DC average of the common mode signal:

$$V_{\text{TX-CM-DC}} = DC_{(avg)} \text{ of } \frac{|V_{\text{TX-D+}} + V_{\text{TX-DC-}}|}{2}$$

NOTE The base specification states that $V_{TX-DC-CM}$ must be held at the same value during all states. For complete validation, this measurement should be performed on the device in all states and the results compared.

Test References

Table 88 Avg DC Common Mode Output Voltage Test References

Test Name	Reference	PCI-SIG Assertions
Avg DC Common Mode Output Voltage	PCI Express Base Specification, Rev 1.1, Table 4-5	PHY.3.1#12

DC Common Mode Line Delta

Table 89 $V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$ from Table 4-5 of the Base Specification

Symbol	Parameter	Min	Nom	Max
$V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0 V		25 mV

Test Definition Notes from the Specification

- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured using the clock recovery function specified in Section 4.3.3.2. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).

Limits

$0\ \text{V} < V_{TX\text{-}CM\text{-}LINE\text{-}DELTA} \leq 25\text{mV}$

Test Procedure

Follow the procedure in "Running Common Mode Voltage Tests" on page 129, and select "DC Common Mode Line Delta".

NOTE

This test is only available when the single-ended or SMA probing method has been used (see "Probing the Link for Tx Compliance" on page 112).

Measurement Algorithm

$$\left|V_{\text{TX-CM-DC-D+}} - V_{\text{TX-DM-DC-D-}}\right| \leq 25\ \text{mV}$$

$$V_{\text{TX-CD-DC-D+}} = DC_{(avg)}\ \text{of}\ \left|V_{\text{TX-D+}}\right|$$

$$V_{\text{TX-CD-DC-}} = DC_{(avg)}\ \text{of}\ \left|V_{\text{TX-D-}}\right|$$

Test References

Table 90 DC Common Mode Line Delta Test References

Test Name	Reference	PCI-SIG Assertions
DC Common Mode Line Delta	PCI Express Base Specification, Rev 1.1, Table 4-5	PHY.3.1#26

DC Common Mode Output Voltage Variation

Test Definition Notes from the Specification

The TX DC common mode voltage ($V_{TX\text{-}DC\text{-}CM}$) must be held at the same value during all states. The allowable range for $V_{TX\text{-}DC\text{-}CM}$ is 0 to 3.6 V (±100 mV).

Limits

$|V_{TX\text{-}DC\text{-}CM\text{-}VARIATION}| \leq 100$ mV

Test Procedure

Follow the procedure in "Running Common Mode Voltage Tests" on page 129, and select "DC Common Mode Output Voltage Variation".

NOTE This test is only available when the single-ended or SMA probing method has been used (see "Probing the Link for Tx Compliance" on page 112).

Measurement Algorithm

The Tx DC Common Mode Output Voltage Variation measurement computes the worst case positive or negative excursion of the common mode signal from the average DC Common Mode Voltage $V_{TX\text{-}DC\text{-}CM}$

$$V_{TX\text{-}DC\text{-}CM\text{-}VARIATION} = | \text{Max}(\text{Max}(V_{CM(i)}), \text{Min}(V_{CM(i)})) - V_{TX\text{-}DC\text{-}CM} |$$

Where:

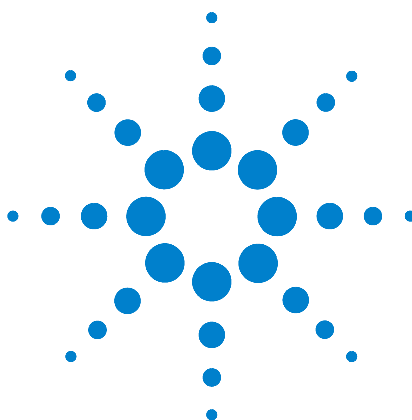
i is the index of all waveform values.

V_{CM} is the common mode signal $(V_{TX\text{-}D+} + V_{TX\text{-}D-})/2$.

Test References

Table 91 DC Common Mode Output Voltage Variation Test References

Test Name	Reference	PCI-SIG Assertions
DC Common Mode Output Voltage Variation	PHY ELECTRICAL TEST CONSIDERATIONS, REVISION 1.0RD, Section 4.1.6	PHY.3.1#12



9
Transmitter (Tx) Tests, PCI-E 1.1, Low Power

Probing the Link for Tx Compliance 139
Tx Compliance Test Load 139
Running Signal Quality Tests 139
Running Common Mode Voltage Tests 142

This section provides the Methods of Implementation (MOIs) for Transmitter tests using an Agilent 54855A, 80000B, or 90000A series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

The *Mobile Graphic Low Power Addendum to The PCIE Base Specification 1.0* is applicable to PCIE 1.1 as well.

PCIE 1.1 Low Power Transmitter Tests consist of all tests from PCIE 1.1 Full (Standard) Power Tests except de-emphasis tests. The following table shows all the PCIE 1.1 Low Power Tests:

Table 92 PCIE 1.1 Low Power Transmitter Tests

Test Name	Remarks	See
Unit Interval	Same as Full Power	page 118.
Template Tests	Different	page 140.
Median to Max Jitter	Different	page 141.
Eye-Width	Different	page 141.
Peak Differential Output Voltage	Different	page 141.
Rise/Fall Time	Same as Full Power	page 126.
RMS AC Peak Common Mode Output Voltage	Same as Full Power	page 130.
Avg DC Common Mode Output Voltage	Same as Full Power	page 132.
DC Common Mode Output Voltage Variation	Same as Full Power	page 135.
DC Common Mode Line Delta	Same as Full Power	page 134.

All the tests above remarked with “Same as Full Power” share the same Method of Implementation (MOI) with PCIE 1.1 Full Power (refer to the page numbers shown). The differences in the test method are described in this chapter.

Probing the Link for Tx Compliance

When performing low-power transmitter tests, probing is the same as for full-power tests. See “Probing the Link for Tx Compliance" on page 112.

Tx Compliance Test Load

When performing low-power transmitter tests, the compliance test load is the same as for full-power tests. See “Tx Compliance Test Load" on page 116.

Running Signal Quality Tests

Start the automated testing application as described in “Starting the PCI Express Automated Test Application" on page 22. Then, when selecting tests, navigate to “Signal Quality” in the “Transmitter (Tx) Tests” group.

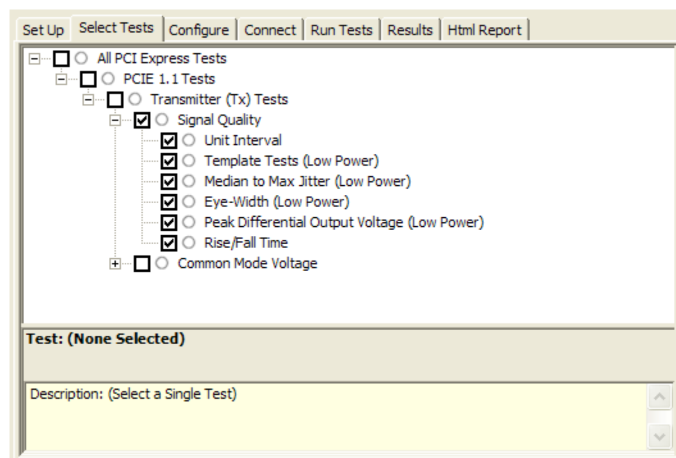


Figure 39 Selecting Transmitter (Tx) Signal Quality Tests

Unit Interval

When performing low-power transmitter tests, the Tx Unit Interval test is the same as for full-power tests. See “Unit Interval" on page 118.

Template Tests (Low Power)

Test Definition/Reference

Mobile Graphics Low-Power Addendum to the PCI Express Base Specification 1.0

- Compliance of the transmitter eye diagram uses the same methodology as outlined in PCI Express Base 1.0a. The Tx eye diagram is specified using the passive compliance/test measurement load (see Figure 2-1 of Mobile Low Power PCIE Specification) in place of any real PCI Express interconnect plus Rx component. Because de-emphasis is not implemented, the transition and de-emphasized bit transitions are merged into a single Transmitter compliance eye diagram.
- The eye diagram must be valid for any 250 consecutive UIs.
- A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

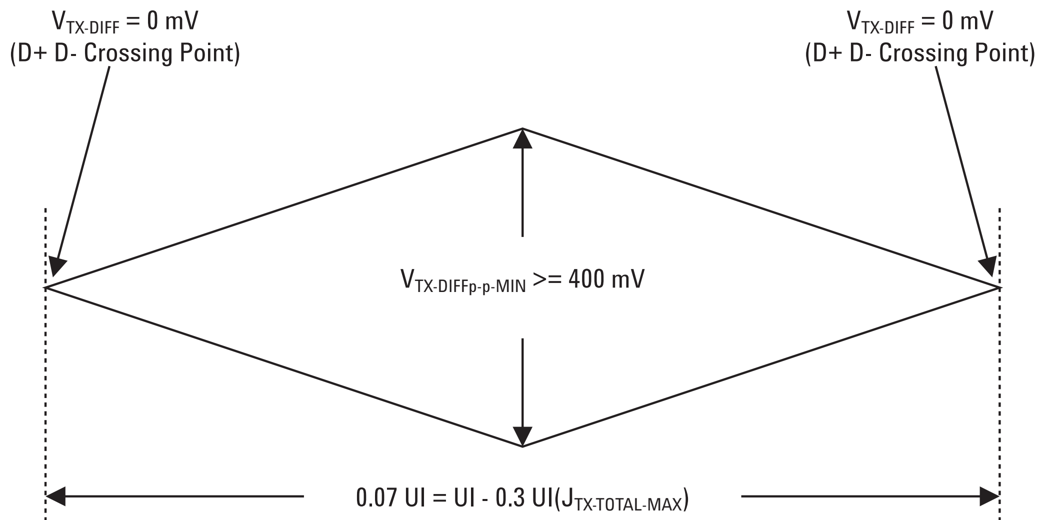


Figure 40 Transmitter Compliance Eye Diagram from Figure 2-2 of the Mobile Graphic Low-Power Addendum.

Difference in Test Procedure Compared to Full Power

- Different Eye diagram used. The Eye diagram can be found in Figure 2.2 of Mobile Low Power PCIE Specification.
- Eye diagram only runs once with both transition and non-transition bits since de-emphasis is no longer needed for low power specification.

See Also “Template Tests" on page 119.

Median to Max Jitter (Low Power)

Difference in Test Procedure Compared to Full Power

- Eye diagram only runs once with both transition and non-transition bits since de-emphasis is no longer needed for low power specification.

See Also "Median to Max Jitter" on page 121.

Eye-Width (Low Power)

Difference in Test Procedure Compared to Full Power

- Eye diagram only runs once with both transition and non-transition bits since de-emphasis is no longer needed for low power specification.

See Also "Eye-Width" on page 123.

Peak Differential Output Voltage (Low Power)

Difference in Test Procedure Compared to Full Power

- Different specification used:

Table 93 $V_{TX-DIFFp-p}$ from Table 2-1 of the Mobile Graphic Low-Power Addendum.

Symbol	Parameter	Min	Nom	Max
$V_{TX-DIFFp-p}$	Differential Pk-Pk Output Voltage	0.400 V		1.2 V

- $V_{TX-DIFFp-p} = 2^*|V_{TX-D+} - V_{TX-D-}|$
- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 2-1 (Mobile Graphic Low Power Addemdum) and measured over any 250 consecutive TX UIs. Also refer to the Transmitter compliance eye diagram shown in Figure 2-2 (Mobile Graphic Low Power Addemdum).

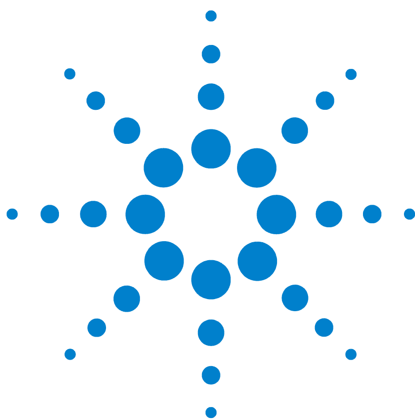
See Also "Peak Differential Output Voltage" on page 125.

Rise/Fall Time

When performing low-power transmitter tests, the Tx Rise/Fall Time test is the same as for full-power tests. See "Rise/Fall Time" on page 126.

Running Common Mode Voltage Tests

When performing low-power transmitter tests, the common mode voltage tests are the same as for full-power tests. See "Running Common Mode Voltage Tests" on page 129.



10
Receiver (Rx) Tests, PCI-E 1.1

Probing the Link for Rx Compliance 144
Running Receiver Tests 147

This section provides the Methods of Implementation (MOIs) for Receiver tests using an Agilent 54855A, 80000B, or 90000A series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

NOTE

None of the included receiver tests validate the receiver's ability to correctly receive data (also known as receiver tolerance). Rather, they validate that the signal as seen by the receiver meets or exceeds various parameters (maximum voltage, jitter, eye width, etc.). These tests validate the transmitter and interconnect. Separate receiver tolerance testing is required to ensure the receiver is correctly receiving data.

Probing the Link for Rx Compliance

Receiver tests are done by probing the link as close as is feasibly possible to the pins of the receiver device. Alternatively, a dummy load can be used for the termination of the link. To probe the receiver link, you can:

- Use two differential probe heads with two 1134A probe amplifiers (with the negative lead grounded for single-ended measurements) and the channel 1 and channel 3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.
- Use one differential probe head with the 1134A probe amplifier and the channel 2 input of an oscilloscope that has 20 GS/s sample rate available on that channel.

Table 94 Probing Options for Receiver Testing

	Probing Configurations			Captured Waveforms		System Specifications	
						54855A	
	Probing Method	Break Serial Link	Channels Used	Differential Mode	Common Mode	System Band Width	Rise* Time (20-80)
DUT Connection	Single-Ended (2 x 1134A w/ Differential Probe Heads)	Y/N	2	Pseudo	Yes	6 GHz	70 ps
	Differential (1 x 1134A w/ Differential Probe Head)	Y/N	1	True	No	6 GHz	70 ps

*Typical

Single-Ended Probing

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Source 1 - Source 2. The Sources can be either channels 1 and 3 or channels 2 and 4. The Common mode measurements are also available in this configuration from the common mode waveform (Source 1 + Source 2)/2.

Make sure to probe equal distances from the receiver, as close as possible to the receiver, with the shortest ground connection possible.

This probing technique can be used for either a live link that is transmitting data, or a link terminated into a “dummy load.”

Channel-to-channel deskew is required using this technique because two channels are used.

For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 392.

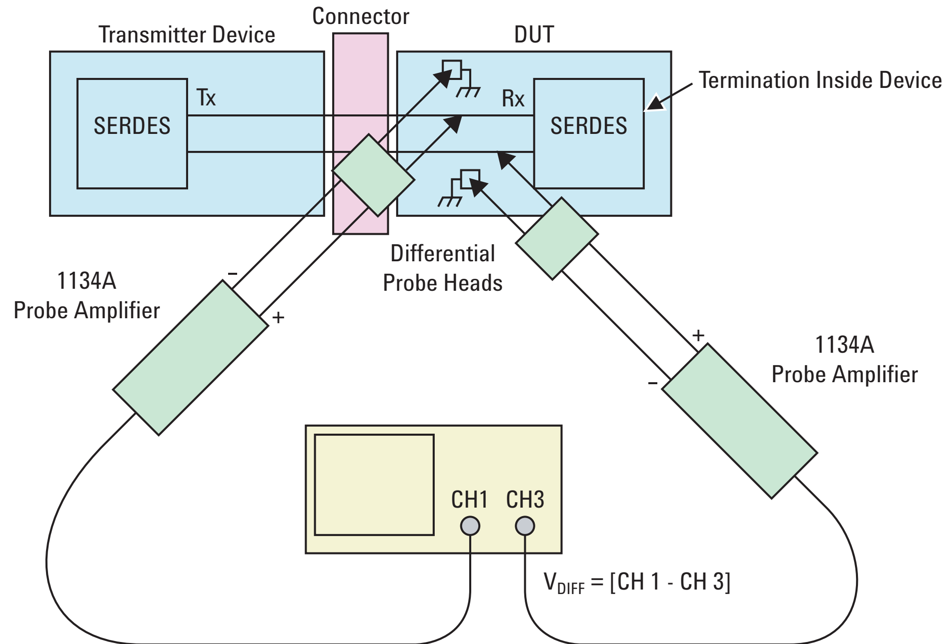


Figure 41 Single-Ended Probing

Differential Probing

The differential signal is measured directly by the differential probe head.

Make sure to probe equal distances from the receiver, as close as possible to the receiver, with the shortest ground connection possible.

This probing technique can be used for either a live link that is transmitting data, or a link terminated into a “dummy load.”

A single channel of the oscilloscope is used, so de-skew is not necessary.

For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 392.

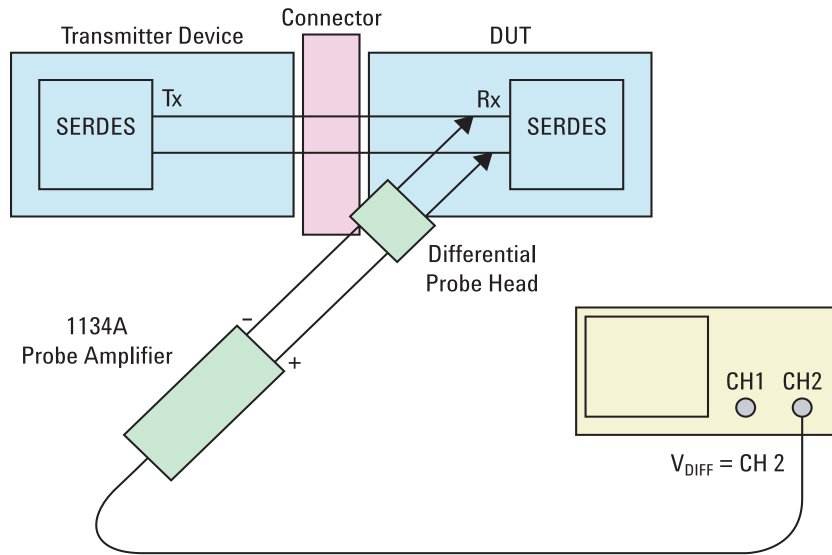


Figure 42 Differential Probing

Running Receiver Tests

Start the automated testing application as described in “Starting the PCI Express Automated Test Application" on page 22. Then, when selecting tests, navigate to the “Receiver (Rx) Tests” group.

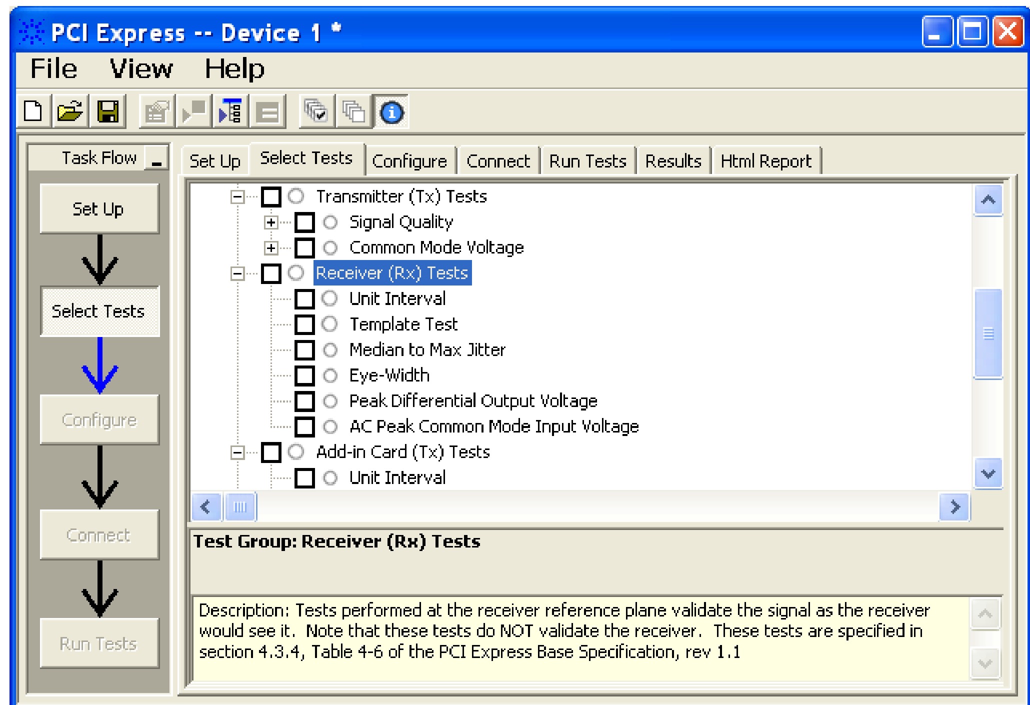


Figure 43 Selecting Receiver (Rx) Tests

Unit Interval

Table 95 UI from Table 4-6 of the Base Specification

Symbol	Parameter	Min	Nom	Max
UI	Unit Interval	399.88 ps	400ps	400.12 ps

Refer to “Tx, Unit Interval" on page 257. The MOI for the measurement of UI at the receiver is identical to measuring it at the transmitter, with the exception of the test point.

Test References

Table 96 Unit Interval Test References

Test Name	Reference	PCI-SIG Assertions
Unit Interval	PCI Express Base Specification, Rev 1.1, Table 4-6	

Test Definition Notes from the Specification

- UI (Unit Interval) is specified to be ±300 ppm.
- UI does not account for SSC dictated variations.
- No test load is necessarily associated with this value.

Template Test

See Section 4.3.4 of the Base Specification for additional notes and test definitions.

Test Definition Notes from the Specification

- The RX eye diagram in Figure 4-26 of the Base Specification is specified using the passive compliance/test measurement load (see Figure 4-25, Base Specification) in place of any real PCI Express RX component.

NOTE In general, the minimum Receiver eye diagram measured with the compliance/test measurement load (see Figure 4-25, Base Specification) will be larger than the minimum Receiver eye diagram measured over a range of systems at the input Receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input Receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 4-26, Base Specification) expected at the input Receiver based on some adequate combination of system simulations and the Return Loss measured looking into the RX package and silicon.

- The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.
- The eye diagram must be valid for any 250 consecutive UIs.

- A recovered RX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the RX UI.

Test Procedure

Follow the procedure in "Running Receiver Tests" on page 147, and select "Template Test".

Test References

Table 97 Template Test References

Test Name	Reference	PCI-SIG Assertions
Template Test	PCI Express Base Specification, Rev 1.1, Figure 4-26	PHY.3.4#1

Median to Max Jitter

Table 98 $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ from Table 4-6 of the Base Specification

Symbol	Parameter	Min	Nom	Max
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.			0.3 UI

Test Definition Notes from the Specification

- Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to the recovered TX UI to be measured after the clock recovery function in Section 4.3.3.2.
- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured using the clock recovery function specified in Section 4.3.3.2. Also refer to the Transmitter compliance eye diagram shown in Figure 4-26 (Base Specification). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered using the clock recovery function specified in Section 4.3.3.2 must be used as a reference for the eye diagram.

- The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total 0.64. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. The RX UI recovered using the clock recovery function specified in Section 4.3.3.2 must be used as the reference for the eye diagram. The T_{RX-EYE} measurement is to be met at the target bit error rate. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ is to be met using the compliance pattern at a sample size of 1,000,000 UI.

Limits

Maximum = 0.3 UI

Pass Condition

0.3 UI > $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$.

Test Procedure

Follow the procedure in “Running Receiver Tests" on page 147, and select “Median to Max Jitter”.

Measurement Algorithm

Refer to “Median to Max Jitter" on page 149 for Rx Median-to-Max Jitter measurement algorithm.

Test References

Table 99 Median to Max Jitter Test References

Test Name	Reference	PCI-SIG Assertions
Median to Max Jitter	PCI Express Base Specification, Rev 1.1, Table 4-6	PHY.3.4#6

Eye-Width

Table 100 T_{RX-EYE} from Table 4-6 of the Base Specification

Symbol	Parameter	Min	Nom	Max
T_{RX-EYE}	Minimum Receiver Eye Width	0.4 UI		

Test Definition Notes from the Base Specification

- The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI.
- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured using the clock recovery function specified in Section 4.3.3.2. Also refer to the Transmitter compliance eye diagram shown in Figure 4-26 (Base Specification). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered using the clock recovery function specified in Section 4.3.3.2 must be used as a reference for the eye diagram.
- The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total 0.64. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. The RX UI recovered using the clock recovery function specified in Section 4.3.3.2 must be used as the reference for the eye diagram. The T_{RX-EYE} measurement is to be met at the target bit error rate. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ is to be met using the compliance pattern at a sample size of 1,000,000 UI.
- See the “PCI Express Jitter and BER” white paper for more details on the Rx-Eye measurement.

Limits

Minimum = 0.40 UI

Pass Condition

0.40UI < T_{RX-EYE}.

Test Procedure

Follow the procedure in “Running Receiver Tests" on page 147, and select “Eye-Width”.

Measurement Algorithm

Refer to “Eye-Width" on page 150 for Eye Width measurement algorithm.

Test References

Table 101 Eye-Width Test References

Test Name	Reference	PCI-SIG Assertions
Eye-Width	PCI Express Base Specification, Rev 1.1, Table 4-6	PHY.3.4#1

Peak Differential Output Voltage

Table 102 $T_{RX-DIFFp-p}$ from Table 4-6 of the Base Specification

Symbol	Parameter	Min	Nom	Max
$V_{RX-DIFFp-p}$	Differential Input Peak to Peak Voltage	0.175 V		1.200 V

Test Definition Notes from the Specification

- $V_{RX-DIFFp-p} = 2*|V_{RX-D+} - V_{RX-D-}|$
- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured using the clock recovery function specified in Section 4.3.3.2. Also refer to the Transmitter compliance eye diagram shown in Figure 4-26 (Base Specification). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered using the clock recovery function specified in Section 4.3.3.2 must be used as a reference for the eye diagram.

Test Procedure

Follow the procedure in “Running Receiver Tests" on page 147, and select “Peak Differential Output Voltage”.

Limits

Minimum = 0.40 UI and Maximum = 1.200 V

Pass Condition

$0.175\ V < V_{RX-DIFFp-p} < 1.200\ V$

Measurement Algorithm

Refer to “Peak Differential Output Voltage" on page 152 for Differential Voltage measurement algorithms.

NOTE

For receiver testing, Eye Height is measured on all UIs.

Test References

Table 103 Peak Differential Output Voltage Test References

Test Name	Reference	PCI-SIG Assertions
Peak Differential Output Voltage	PCI Express Base Specification, Rev 1.1, Table 4-6	PHY.3.4#1

AC Peak Common Mode Input Voltage

Table 104 $V_{RX\text{-}CM\text{-}ACp}$ from Table 4-6 of the Base Specification

Symbol	Parameter	Min	Nom	Max
$V_{RX\text{-}CM\text{-}ACp}$	AC Peak Common Mode Input Voltage			150 mV

Test Definition Notes from Specification

- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured using the clock recovery function specified in Section 4.3.3.2. Also refer to the Transmitter compliance eye diagram shown in Figure 4-26 (Base Specification). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered using the clock recovery function specified in Section 4.3.3.2 must be used as a reference for the eye diagram.

Limits

Maximum = 150 mV

Pass Condition

150 mV > $V_{RX\text{-}CM\text{-}ACp}$.

Test Procedure

Follow the procedure in “Running Receiver Tests" on page 147, and select “AC Peak Common Mode Input Voltage”.

Measurement Algorithms

This measurement is made over 250 consecutive bits defined in Section 3.4 of the Base Specification.

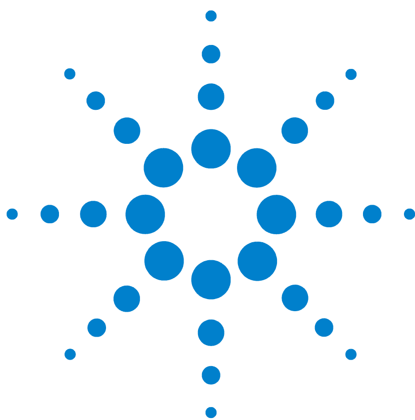
$$V_{\text{RX-CM-AC}} = \frac{|V_{\text{RX-D+}} + V_{\text{RX-D-}}|}{2} - V_{\text{RX-CM-DC}}$$

$$V_{\text{RX-CM-DC}} = DC_{(avg)} \text{ of } \frac{|V_{\text{RX-D+}} + V_{\text{RX-D-}}|}{2}$$

Test References

Table 105 AC Peak Common Mode Input Voltage Test References

Test Name	Reference	PCI-SIG Assertions
AC Peak Common Mode Input Voltage	PCI Express Base Specification, Rev 1.1, Table 4-6	PHY.3.4#2



11
Add-In Card (Tx) Tests, PCI-E 1.1

Probing the Link for Add-In Card Compliance 156
Running Add-In Card Tests 159

This section provides the Methods of Implementation (MOIs) for Add-In Card Transmitter tests using an Agilent 54855A, 80000B, or 90000A series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

Probing the Link for Add-In Card Compliance

Connecting the Signal Quality Load Board for Add-in Card Testing

There are multiple pairs of SMA connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1 With the Add-in card fixture power supply powered off, connect the power supply connector to the Add-in card test fixture, and connect the device under test add-in card to the by-16 or by-1 connector slot.

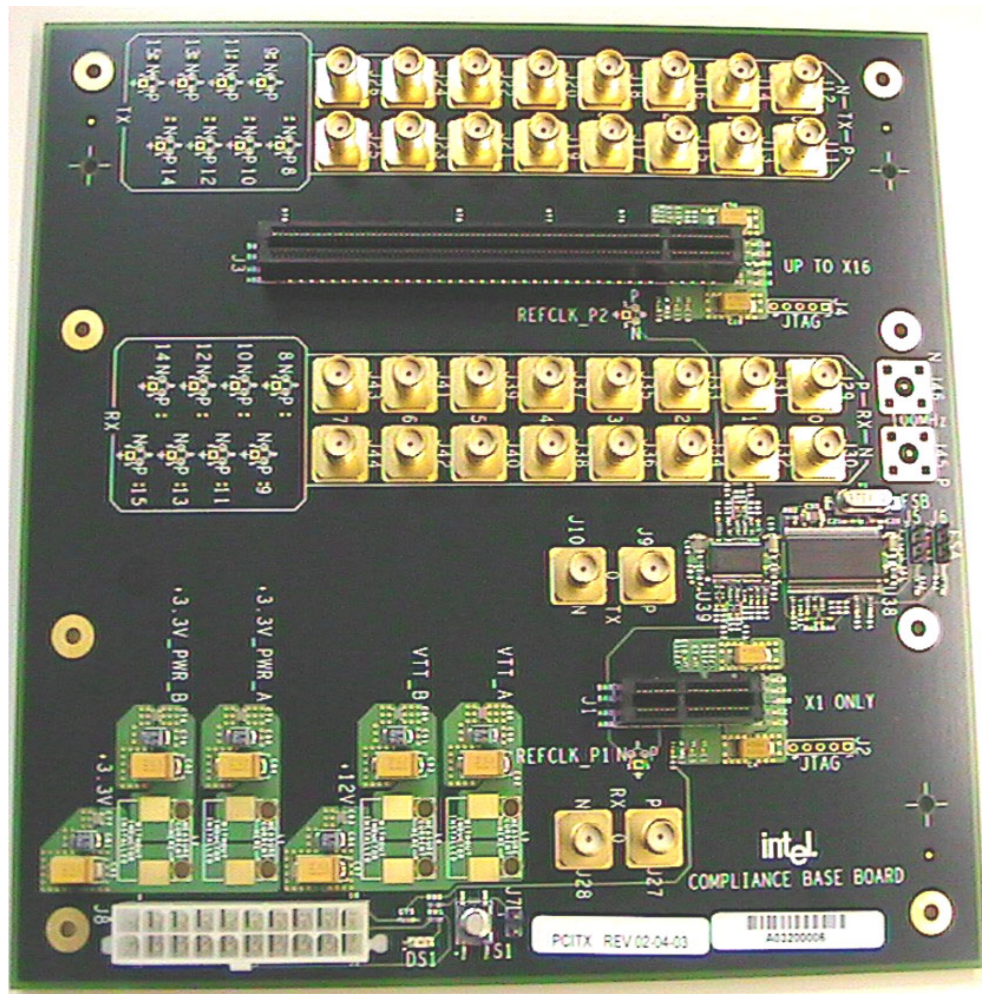


Figure 44 Compliance Base Board (CBB) Add-in Card Fixture

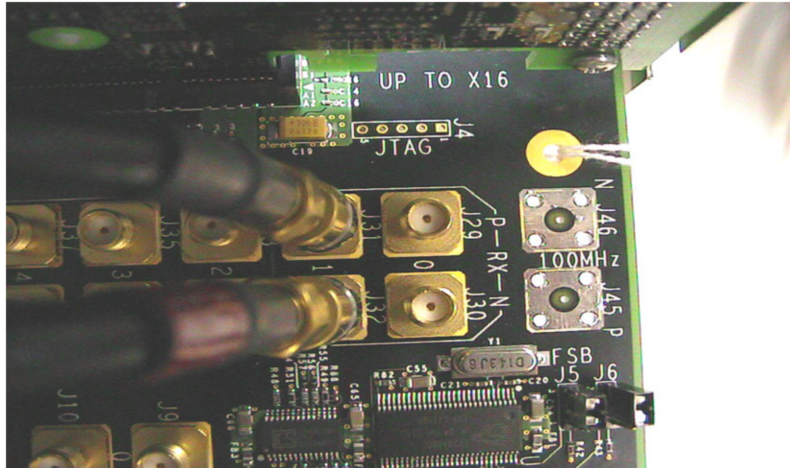


Figure 45 Compliance Base Board (CBB) SMA Probing Option

2 Connect cables up as follows:

   a Digital Storage Oscilloscope channel 1 to the TX LANE P under test (where Lane 1 is under test in this example shown in Figure 45 above).

   b Digital Storage Oscilloscope channel 3 to the TX LANE N under test (where Lane 1 is under test in this example shown in Figure 45 above).

NOTE The Compliance Base Board labeled PCITX Rev 02-04-03 silk screen incorrectly labels the add-in card transmitter probing locations as RX.

When SMA probing and two channels are used, channel-to-channel deskew is required (see “Channel-to-Channel De-skew" on page 386).

Not all lanes have SMA probing options. For signal quality testing of the remaining lanes you will need to use a high bandwidth differential or single ended probes (see Figure 46 on page 158). For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 392.

When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the 1134A probe amplifier.

When using a single differential probe head, use oscilloscope channel 2.

3 Connect adequate load to the power supply to assure it is regulating and turned on. Generally, one IDE hard drive will provide adequate load.

4 Turn on the power supply. DS1 LED (located near the ATX power supply connector) should turn on. If the LED is on, but the power supply does not turn on, check that the jumper J7 is installed between J7-1 and J7-2.

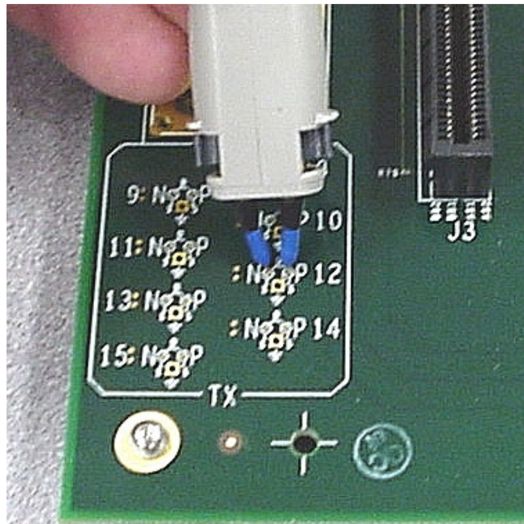


Figure 46 Compliance Base Board (CBB) Active Probing Option

Running Add-In Card Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 22. Then, when selecting tests, navigate to the "Add-In Card (Tx) Tests" group.

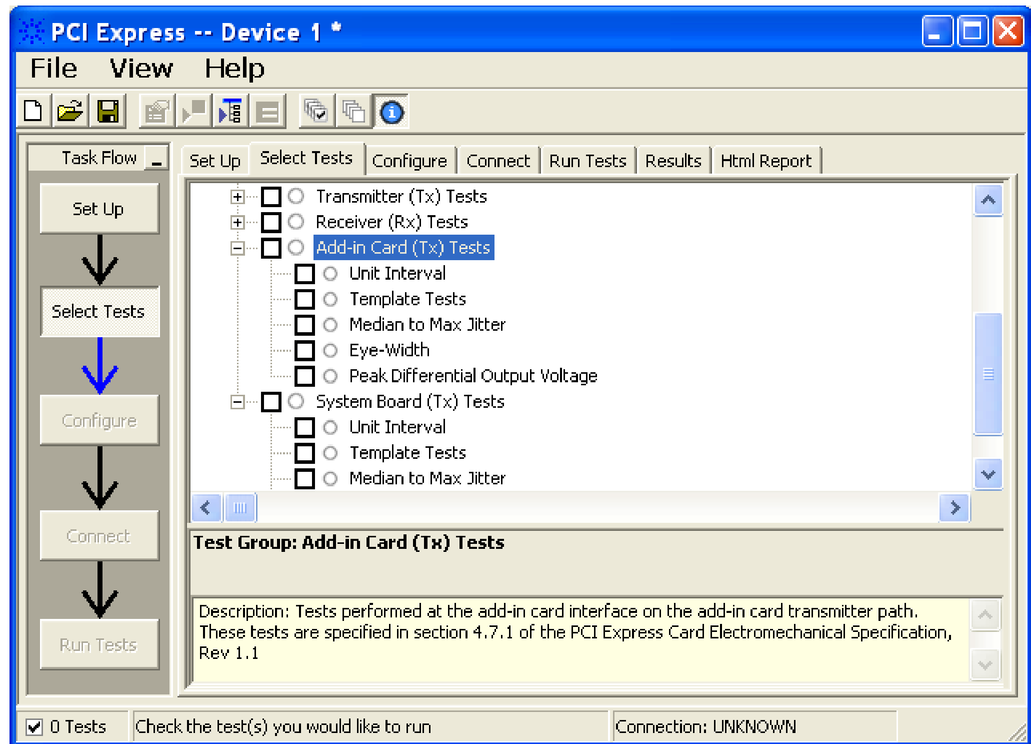


Figure 47 Selecting Add-In Card (Tx) Tests

Unit Interval

Table 106 UI from Table 4-5 of the Base Specification

Symbol	Parameter	Min	Nom	Max
UI	Unit Interval	399.88 ps	400ps	400.12 ps

Test Definition Notes from the Specification

- UI (Unit Interval) is specified to be ±300 ppm.
- UI does not account for SSC dictated variations.

Test Procedure

Follow the procedure in “Running Add-In Card Tests" on page 159, and select “Unit Interval”.

Pass Condition

399.88ps ≤ UI ≤ 400.12ps

Measurement Algorithm

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window.

TX UI(p) = Mean(UI(n))

Where:

n is the index of UI in the clock recovery window.

p indicates the pth 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI, as described below.

NOTE The UI measurement is not required at this point. It is provided as an informative test only.

NOTE The TX UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another TX UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case TX UI is reported.

Test References

Table 107 Unit Interval Test References

Test Name	Reference	PCI-SIG Assertions
Unit Interval	This test is not required. It is informative only.	

Template Tests

See Section 4.7.1 of the Card Electromechanical Specification for additional notes and test definitions.

Test Definition Notes from the Specification

Table 108 Table 4-6 of the Card Electromechanical Specification.

Parameter	Value	Notes
V_{TXA}	≥ 514 mV	All Links are assumed active while generating this eye diagram. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (T_{TXA_d}).
V_{TXA_d}	≥ 360 mV	
T_{TXA}	≥ 287 ps	

- An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage lever (V_{TXA_d}). V_{TXA} and V_{TXA_d} are differential peak-to-peak output voltages.
- T_{TXA} is the minimum eye width. The sample size for this measurement is 10^6 UI. This value can be reduced to 274 ps for simulation purposes at a BER of 10^{-12}.
- The values in Table 108 are referenced to an ideal 100 ohm differential load at the end of the interconnect path at the edge-finger boundary on the add-in card. The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the “PHY Electrical Test Considerations for PCI Express Architecture” document.

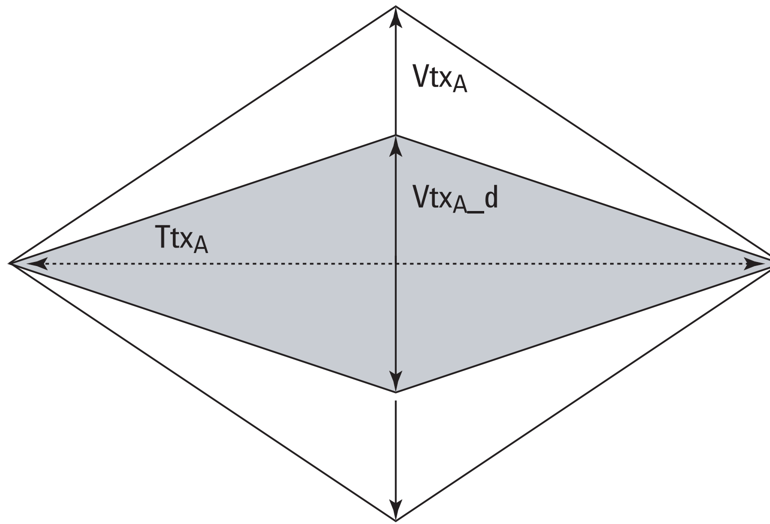


Figure 48 Compliance Eye Diagram

Test References

Table 109 Template Tests Test References

Test Name	Reference	PCI-SIG Assertions
Template Tests	PCI Express CEM Specification, Rev 1.1, Section 4.7.1, Figure 4-8	EM.4#19

Median to Max Jitter

Table 110 $J_{TX-A-MEDIAN-to-MAX-JITTER}$ for Add-In Card

Symbol	Parameter	Min	Nom	Max
$J_{TXA-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.			56.5 ps

Test Definition Notes from the Specification

- An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram.
- $J_{TXA-MDEDIAN-to-MAX-JITTER}$ is the maximum median-to-peak jitter outlier as defined in the “PCI Express Base Specification, Revision 1.1.” The sample size for this measurement is 10^6 UI. This value can be increased to 63 ps for simulation purposes at a BER of 10^{-12}.
- The values in Table 110 are referenced to an ideal 100 ohm differential load at the end of the interconnect path at the edge-finger boundary on the add-in card. The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the “PHY Electrical Test Considerations for PCI Express Architecture” document.

Limits

Maximum = 56.5 ps

Pass Condition

$56.5 \text{ ps} \leq T_{TXA-MEDIAN-to-MAX-JITTER}$

Test Procedure

Follow the procedure in “Running Add-In Card Tests" on page 159, and select “Median to Max Jitter”.

Test References

Table 111 Median to Max Jitter Test References

Test Name	Reference	PCI-SIG Assertions
Median to Max Jitter	PCI Express CEM Specification, Rev 1.1, Table 4-7	EM.4#13, EM.4#19

Eye-Width

Table 112 T_{TXA} for Add-In Card

Symbol	Parameter	Min	Nom	Max
T_{TXA}	Minimum TX Eye Width	287 ps		

Test Definition Notes from the Specification

- An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram.
- $J_{TXA-MEDIAN-to-MAX-JITTER}$ is the maximum median-to-peak jitter outlier as defined in the “PCI Express Base Specification, Revision 1.1.” The sample size for this measurement is 10^6 UI. This value can be increased to 274 ps for simulation purposes at a BER of 10^{-12}.
- The values in Table 112 are referenced to an ideal 100 ohm differential load at the end of the interconnect path at the edge-finger boundary on the add-in card. The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the “PHY Electrical Test Considerations for PCI Express Architecture” document.
- T_{TXA} is the minimum eye width. The sample size for this measurement is 10^6 UI. This value can be reduced to 274 ps for simulation purposes at a BER of 10^{-12}.

NOTE

The median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

Limits

Minimum = 287 ps

Pass Condition

287 ps ≤ T_{TXA}

Test Procedure

Follow the procedure in “Running Add-In Card Tests" on page 159, and select “Eye-Width”.

Test References

Table 113 Eye-Width Test References

Test Name	Reference	PCI-SIG Assertions
Eye-Width	PCI Express CEM Specification, Rev 1.1, Table 4-7	EM.4#13, EM.4#19

Peak Differential Output Voltage

Table 114 $V_{TX\text{-}DIFFp\text{-}p}$ for Add-in Card

Symbol	Parameter	Min	Nom	Max
$V_{TX\text{-}DIFFp\text{-}p}$	Differential Pk-Pk Output Voltage	0.8 V		1.2 V

Test Definition Notes from the Specification

- This is the ration of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition.
- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 of the Base Specification and measured using the clock recovery function specified in Section 4.3.3.2. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 of the Base Specification.

Test Procedure

Follow the procedure in “Running Add-In Card Tests" on page 159, and select “Peak Differential Output Voltage”.

Pass Condition

$0.8\ V \leq V_{TX\text{-}DIFF\text{-}p\text{-}p} \leq 1.2V$

Measurement Algorithm

The Differential Peak Voltage measurement returns two times the larger of the Min or Max statistic if the differential voltage waveform.

$$V_{TX\text{-}DIFF\text{-}p\text{-}p} = 2*Max(Max(V_{DIFF(i)}), Min(V_{DIFF(i)}))$$

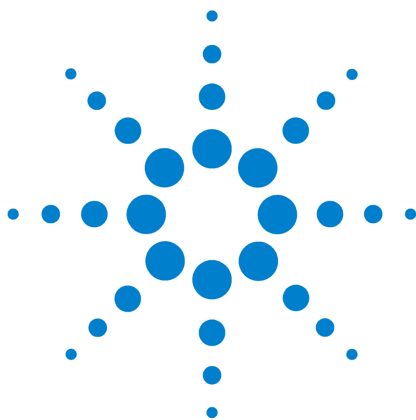
Where:

i is the index of all waveform values.
V_{DIFF} is the Differential Voltage signal.

Test References

Table 115 Peak Differential Output Voltage Test References

Test Name	Reference	PCI-SIG Assertions
Peak Differential Output Voltage	PCI Express Base Specification, Rev 1.1, Table 4-5	EM.4#19



12
System Board (Tx) Tests, PCI-E 1.1

Probing the Link for System Board Compliance 170
Running System Board Tests 172

This section provides the Methods of Implementation (MOIs) for System Board Transmitter tests using an Agilent 54855A, 80000B, or 90000A series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

Probing the Link for System Board Compliance

Connecting the Signal Quality Load Board for System/Motherboard Testing

There are multiple pairs of SMA connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1 With the system/motherboard powered off, connect the Compliance PCI Express Signal Quality Load Board into the connector under test. The PCI Express Signal Quality Load Board has edge fingers for x1, x4, x8 and x16 connectors.

   The PCI Express Signal Quality Load Board will cause a PCI Express 1.1 Base Specification System/motherboard to enter the compliance sub-state of the polling state. During this state the device under test will repeatedly send out the compliance pattern defined in the PCI Express Base Specification.

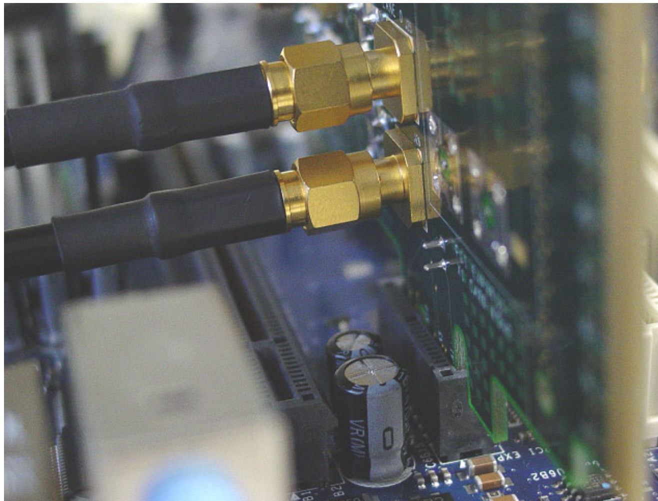


Figure 49 SMA Probing Option

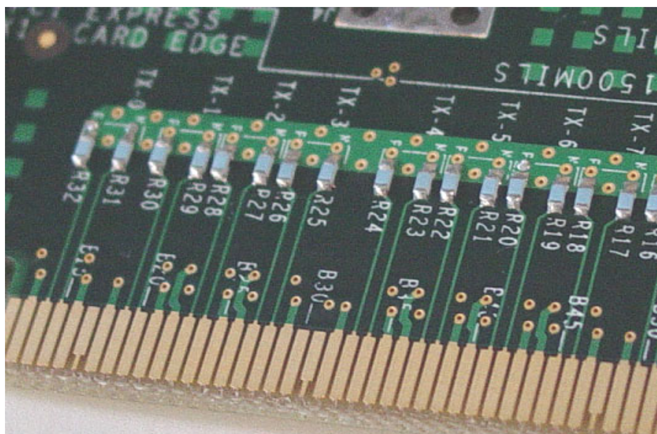


Figure 50 Resistor Terminations for Lanes without SMA Probing

2 Connect cables up as follows:

   a Digital Storage Oscilloscope channel 1 to TX LANE 1 P (where Lane 1 is under test).

   b Digital Storage Oscilloscope channel 3 to TX LANE 1 N (where Lane 1 is under test).

When SMA probing and two channels are used, channel-to-channel deskew is required (see “Channel-to-Channel De-skew" on page 386).

Not all lanes have SMA probing options. For signal quality testing of the remaining lanes you will need to use a high bandwidth differential or single ended probes (see Figure 46 on page 158). For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 392.

When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the 1134A probe amplifier.

When using a single differential probe head, use oscilloscope channel 2.

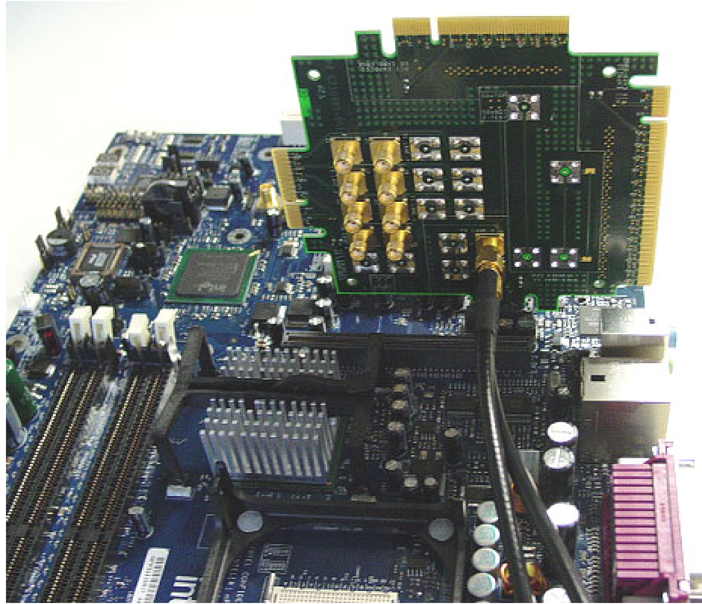


Figure 51 Connecting the PCI Express Signal Quality Test Fixture

Running System Board Tests

Start the automated testing application as described in “Starting the PCI Express Automated Test Application" on page 22. Then, when selecting tests, navigate to the “System Board (Tx) Tests” group.

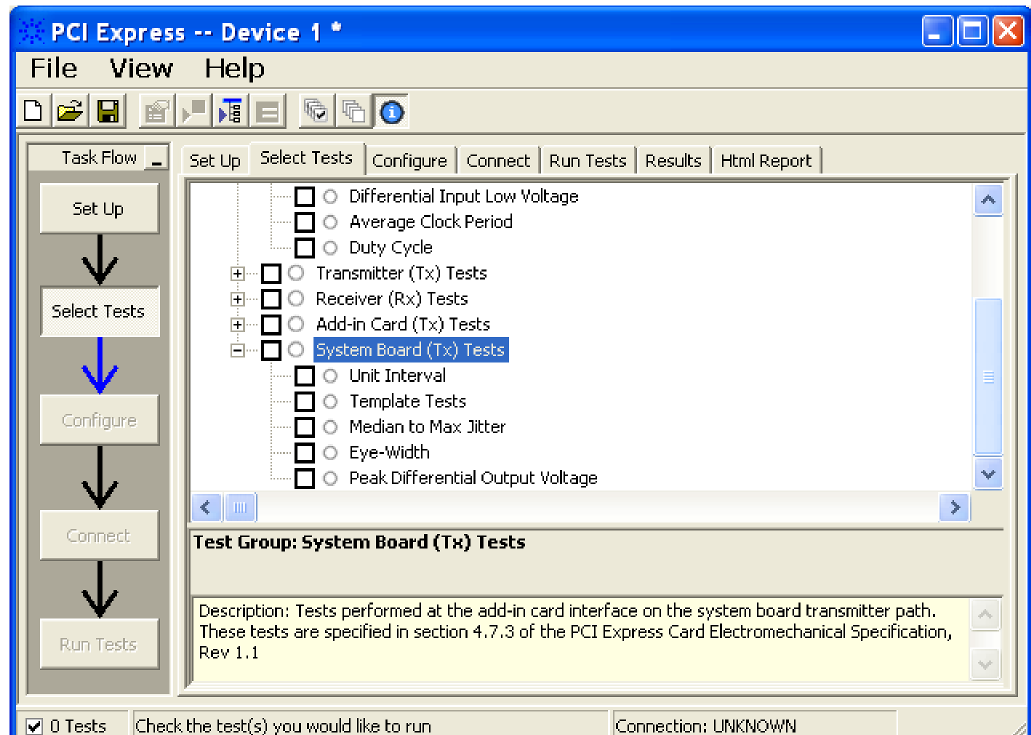


Figure 52 Selecting System Board (Tx) Tests

Unit Interval

Table 116 UI from Table 4-5 of the Base Specification

Symbol	Parameter	Min	Nom	Max
UI	Unit Interval	399.88 ps	400ps	400.12 ps

Test Definition Notes from the Specification

- UI (Unit Interval) is specified to be ±300 ppm.
- UI does not account for SSC dictated variations.

Test Procedure

Follow the procedure in "Running System Board Tests" on page 172, and select "Unit Interval".

Pass Condition

$399.88\text{ps} < \text{UI} < 400.12\text{ps}$

Measurement Algorithm

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window.

TX UI(p) = Mean(UI(n))

Where:

n is the index of UI in the clock recovery window.

p indicates the pth 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI, as described below.

NOTE The UI measurement is not required at this point. It is provided as an informative test only.

NOTE The TX UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another TX UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case TX UI is reported.

Test References

Table 117 Unit Interval Test References

Test Name	Reference	PCI-SIG Assertions
Unit Interval	This test is not required. It is informative only.	

Template Tests

See Section 4.7.3 of the Card Electromechanical Specification for additional notes and test definitions.

Test Definition Notes from the Specification

Table 118 Table 4-8 of the Card Electromechanical Specification

Parameter	Value	Notes
V_{TXS}	≥ 274 mV	All Links are assumed active while generating this eye diagram. Transition and nontransition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (T_{TXS_d}).
V_{TXS_d}	≥ 253 mV	
T_{TXS}	≥ 246 ps	

- An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage lever (V_{TXS_d}). V_{TXS} and V_{TXS_d} are differential peak-to-peak output voltages.
- T_{TXS} is the minimum eye width. The sample size for this measurement is 10^6 UI. This value can be reduced to 233 ps for simulation purposes at a BER of 10^{-12}.
- The values in Table 118 are referenced to an ideal 100 ohm differential load at the end of the interconnect path at the isolated edge-finger boundary of an add-in card when mated with a connector. The eye diagram is defined and centered with respect to the jitter median. The jitter median should be calculated across any 250 consecutive UIs. Exact conditions required for verifying compliance while generating this eye diagram are given in the "PHY Electrical Test Considerations for PCI Express Architecture" document.

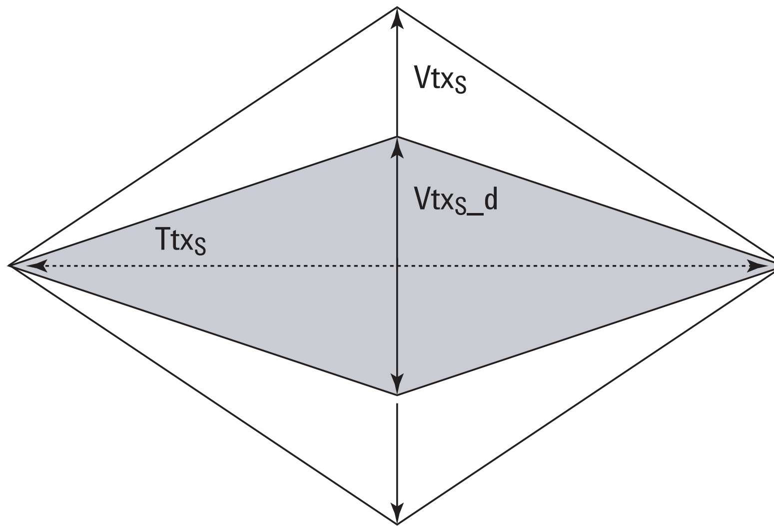


Figure 53 System Board Tx Compliance Eye Diagram

Test References

Table 119 Template Tests Test References

Test Name	Reference	PCI-SIG Assertions
Template Tests	PCI Express CEM Specification, Rev 1.1, Section 4.7.3, Figure 4-10	EM.4#20, EM.4#14

Median to Max Jitter

Table 120 $T_{TXS\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ for System Board

Symbol	Parameter	Min	Nom	Max
$T_{TXS\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	Maximum time between the jitter median and maximum deviation from the median.			77 ps

Test Definition Notes from the Specification

- An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram.
- $J_{TXS\text{-}MDEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ is the maximum median-to-peak jitter outlier as defined in the “PCI Express Base Specification, Revision 1.1.” The sample size for this measurement is 10^6 UI. This value can be increased to 83.5 for simulation purposes at a BER of 10^{-12}.
- The values in Table 120 are referenced to an ideal 100 ohm differential load at the end of the interconnect path at the edge-finger boundary on the add-in card. The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the “PHY Electrical Test Considerations for PCI Express Architecture” document.

Limits

Maximum = 77 ps

Pass Condition

77 ps > $T_{TXS\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$.

Test Procedure

Follow the procedure in “Running System Board Tests" on page 172, and select “Median to Max Jitter”.

Measurement Algorithm

This measurement is made over 250 consecutive bits defined in Section 3.4 of the Base Specification.

The measured time difference between a data edge and a recovered clock edge.

$$tie(n) = t_{R\text{-}DAT}(n) - t_{DAT}(n)$$

Where:

t_{DAT} is the original data edge.

$t_{R\text{-}DAT}$ is the recovered data edge (the ideal time of the data edge as defined by the recovered clock around t_{DAT}).

n is the index of all edges in the waveform.

Test References

Table 121 Median to Max Jitter Test References

Test Name	Reference	PCI-SIG Assertions
Median to Max Jitter	PCI Express CEM Specification, Rev 1.1, Table 4-9	EM.4#20, EM.4#14

Eye-Width

Table 122 T_{TXS} for System Board

Symbol	Parameter	Min	Nom	Max
T_{TXS}	Minimum TX Eye Width	246 ps		

Test Definition Notes from the Specification

- An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram.
- $J_{TXS\text{-}MDEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ is the maximum median-to-peak jitter outlier as defined in the “PCI Express Base Specification, Revision 1.1.” The sample size for this measurement is 10^6 UI. This value can be increased to 83.5 for simulation purposes at a BER of 10^{-12}.
- The values in Table 122 are referenced to an ideal 100 ohm differential load at the end of the interconnect path at the edge-finger boundary on the add-in card. The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the “PHY Electrical Test Considerations for PCI Express Architecture” document.
- T_{TXS} is the minimum eye width. The sample size for this measurement is 10^6 UI. This value can be reduced to 233 ps for simulation purposes at a BER of 10^{-12}.

NOTE The median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

Limits

Minimum = 246 ps

Pass Condition

246 ps ≤ Ttx_S.

Test Procedure

Follow the procedure in “Running System Board Tests" on page 172, and select “Eye-Width”.

Test References

Table 123 Eye-Width Test References

Test Name	Reference	PCI-SIG Assertions
Eye-Width	PCI Express CEM Specification, Rev 1.1, Table 4-9	EM.4#20, EM.4#14

Peak Differential Output Voltage

Table 124 $V_{TXS\text{-}DIFFp\text{-}p}$ for System Board

Symbol	Parameter	Min	Nom	Max
$V_{TXS\text{-}DIFFp\text{-}p}$	Differential Pk-Pk Output Voltage	0.253 V		1.200 V

Test Definition Notes from the Specification

- This is the ration of the $V_{TXS\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TXS\text{-}DIFFp\text{-}p}$ of the first bit after a transition.
- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 of the Base Specification and measured using the clock recovery function specified in Section 4.3.3.2. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 of the Base Specification.

Test Procedure

Follow the procedure in “Running System Board Tests" on page 172, and select “Peak Differential Output Voltage”.

Pass Condition

$0.253\ \text{V} \le V_{TX\text{-}DIFF\text{-}p\text{-}p} \le 1.200\ \text{V}$

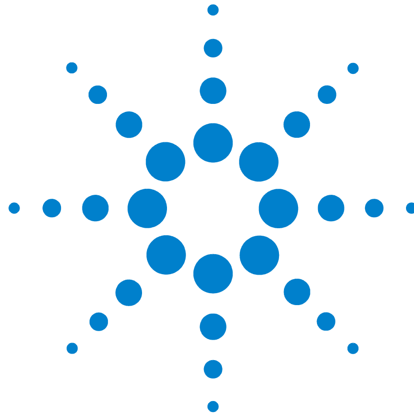
Measurement Algorithm.

$$V_{\text{TXS-DIFFp-p}} = 2 \times \left| V_{\text{TXS-D+}} - V_{\text{TXS-DIFF-}} \right|$$

Test References

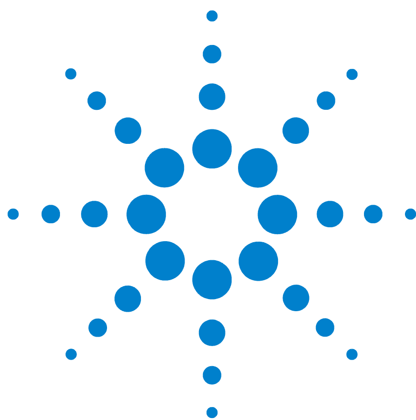
Table 125 Peak Differential Output Voltage Test References

Test Name	Reference	PCI-SIG Assertions
Peak Differential Output Voltage	PCI Express CEM Specification, Rev 1.1, Table 4-9	EM.4#20



Part IV
2.5 GT/s PCI Express Version 2.0

Agilent Technologies



12
Transmitter (Tx) Tests, 2.5 GT/s, PCI-E 2.0, Full Power

Probing the Link for Tx Compliance 184
Tx Compliance Test Load 188
Running Signal Quality Tests 188
Running Common Mode Voltage Tests 201

This section provides the Methods of Implementation (MOIs) for Transmitter tests using an Agilent 54855A, 80000B, or 90000A series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

Probing the Link for Tx Compliance

Transmitter tests are done by connecting the device under test to a test fixture and probing the SMA connectors on the test fixture. To probe the transmitter link, you can:

- Use two 50-ohm coax cables with SMA male connectors, two precision 3.5 mm BNC to SMA male adapters (54855-67604, included with the oscilloscope), and the channel 1 and channel 3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.
- Use two differential probe heads with two 1134A probe amplifiers (with the negative lead grounded for single-ended measurements) and the channel 1 and channel 3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.
- Use one differential probe head with the 1134A probe amplifier and the channel 2 input of an oscilloscope that has 20 GS/s sample rate available on that channel.

When the link is broken and terminated into a 50 ohm load (by the test load), the Compliance Pattern defined in section 4.2.8 (Base Specification) will be transmitted.

Table 126 Probing Options for Transmitter Testing

<table>
<tr><th rowspan="2"></th><th colspan="3">Probing Configurations</th><th colspan="2">Captured Waveforms</th><th colspan="2">Oscilloscope Specifications</th></tr>
<tr><th>Probing Method</th><th>Break Serial Link</th><th>Channels Used</th><th>Differential Mode</th><th>Common Mode</th><th>System Band Width</th><th>Rise* Time (20-80)</th></tr>
<tr><td rowspan="3">DUT Connection</td><td>Single-Ended SMA (2 x 50-Ohm SMA Cables)</td><td>Y</td><td>2</td><td>Pseudo</td><td>Yes</td><td>6 GHz</td><td>70 ps</td></tr>
<tr><td>Single-Ended (2 x 1134A w/ Differential Probe Heads)</td><td>Y/N</td><td>2</td><td>Pseudo</td><td>Yes</td><td>6 GHz</td><td>70 ps</td></tr>
<tr><td>Differential (1 x 1134A w/ Differential Probe Head)</td><td>Y/N</td><td>1</td><td>True</td><td>No</td><td>6 GHz</td><td>70 ps</td></tr>
</table>

*Typical

Single-Ended SMA Probing

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Source 1 - Source 2. The Sources can be either channels 1 and 3 or channels 2 and 4. The Common mode measurements are also available in this configuration from the common mode waveform (Source 1 + Source 2)/2.

This probing technique requires breaking the link and terminating into the 50 ohm/side termination into the oscilloscope. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Channel-to-Channel deskew is required using this technique because two channels are used.

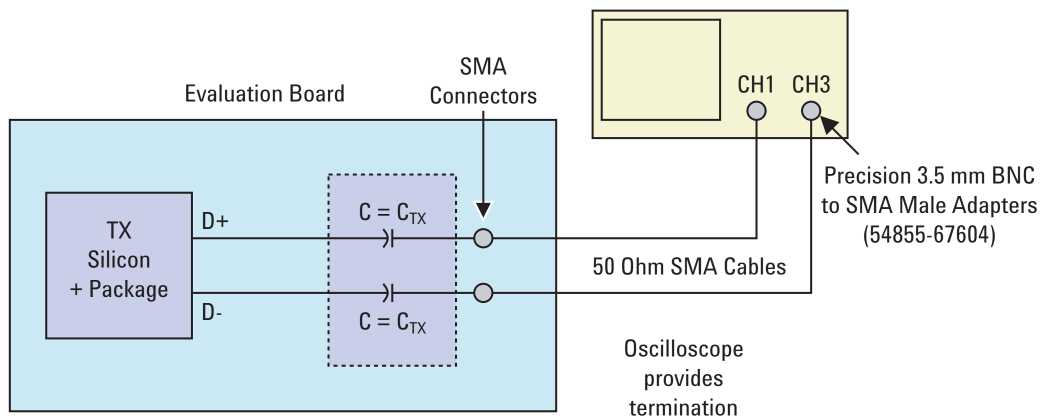


Figure 54 Single-Ended SMA Probing

Single-Ended Probing

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Source 1 - Source 2. The Sources can be either channels 1 and 3 or channels 2 and 4. The Common mode measurements are also available in this configuration from the common mode waveform (Source 1 + Source 2)/2.

Make sure to probe equal distances from the transmitter, as close as possible to the transmitter.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Channel-to-Channel deskew is required using this technique because two channels are used.

For more information on the probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 392.

Place single-ended grounds as close to the signal line’s reference ground as possible.

Figure 55 Single-Ended Probing

Differential Probing

The differential signal is measured directly by the differential probe head.

Make sure to probe equal distances from the transmitter, as close as possible to the transmitter.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Only one channel of the oscilloscope is used.

For more information on the probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 392.

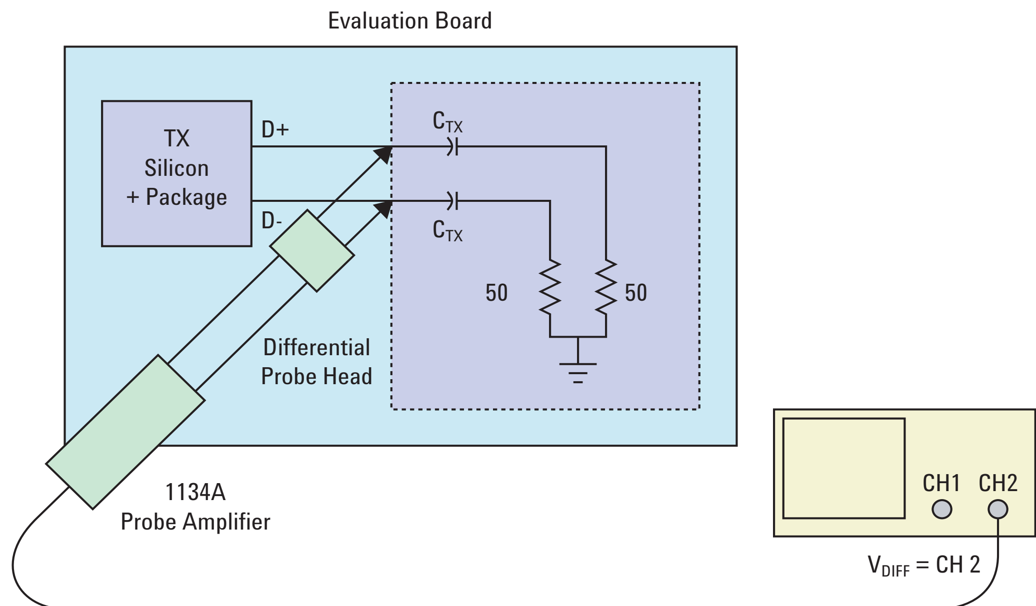


Figure 56 Differential Probing

Tx Compliance Test Load

The compliance test load for driver compliance is shown in Figure 4-25 (Base Specification)

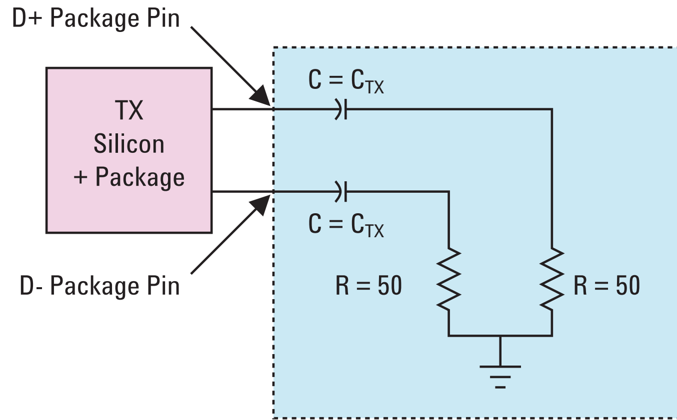


Figure 57 Driver Compliance Test Load.

Running Signal Quality Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 22. Then, when selecting tests, navigate to "Signal Quality" in the "Transmitter (Tx) Tests" group.

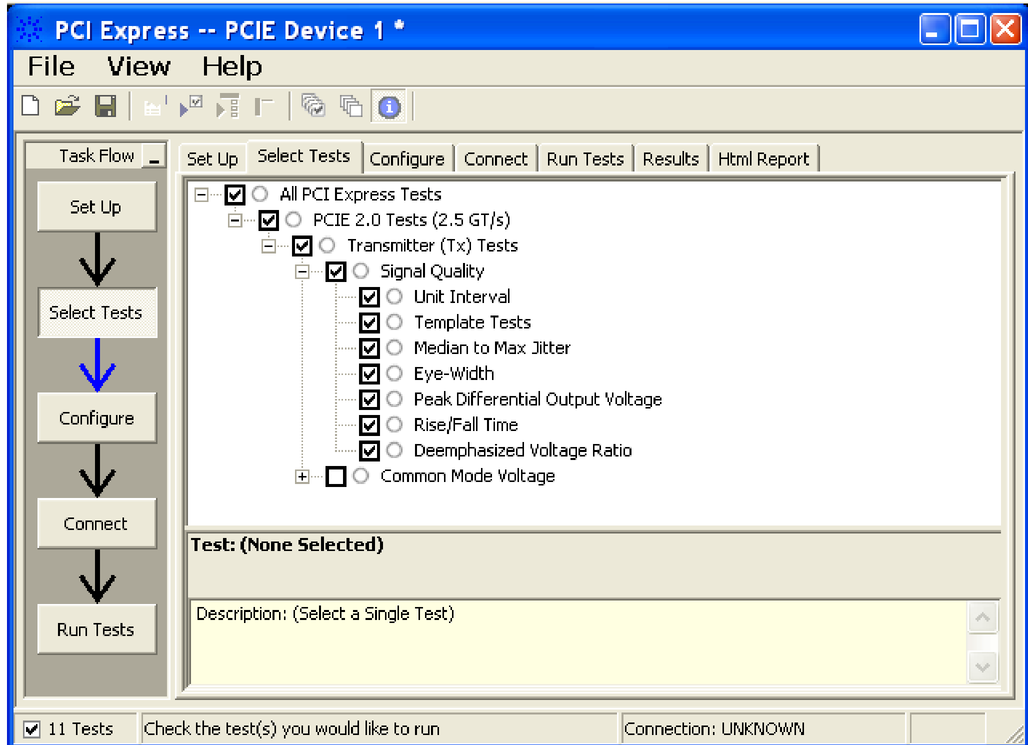


Figure 58 Selecting Transmitter (Tx) Signal Quality Tests

Tx, Unit Interval

Test Definition Notes from the Specification

Table 127 UI from Table 4-9 of the Base Specification: 2.5 and 5.0 GT/s Transmitter Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
UI	Unit Interval	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)	ps	The specified UI is equivalent to a tolerance of ±300 ppm for each Refclk source. Period does not account for SSC induced variations. See Note 1.

NOTE: SSC permits a +0, -5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33 kHz.

- UI is defined in PCI Express Base Specification v2.0, Section 4.3.3.5 and Table 4-9.

Test Procedure

Follow the procedure in “Running Signal Quality Tests" on page 188, and select “Unit Interval”.

Pass Condition

399.88ps < UI < 400.12ps

Measurement Algorithm

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window.

TX UI(p) = Mean(UI(n))

Where:

n is the index of UI in the current 3500 UI clock recovery window.

p indicates the pth 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI, as described below.

NOTE The TX UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another TX UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case TX UI is reported.

Test References

Table 4-9, PCI Express Base Specification v2.0.

Tx, Template Tests

See Section 4.3.3.1 of the Base Specification for additional notes and test definitions.

Test Definition Notes from the Specification

- The TX eye diagram in Figure 4-24 of the Base Specification is specified using the passive compliance/test measurement load in place of any real PCI Express interconnect + RX component.
- There are two eye diagrams that must be met for the Transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.
- The eye diagram must be valid for any 250 consecutive UIs.
- A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

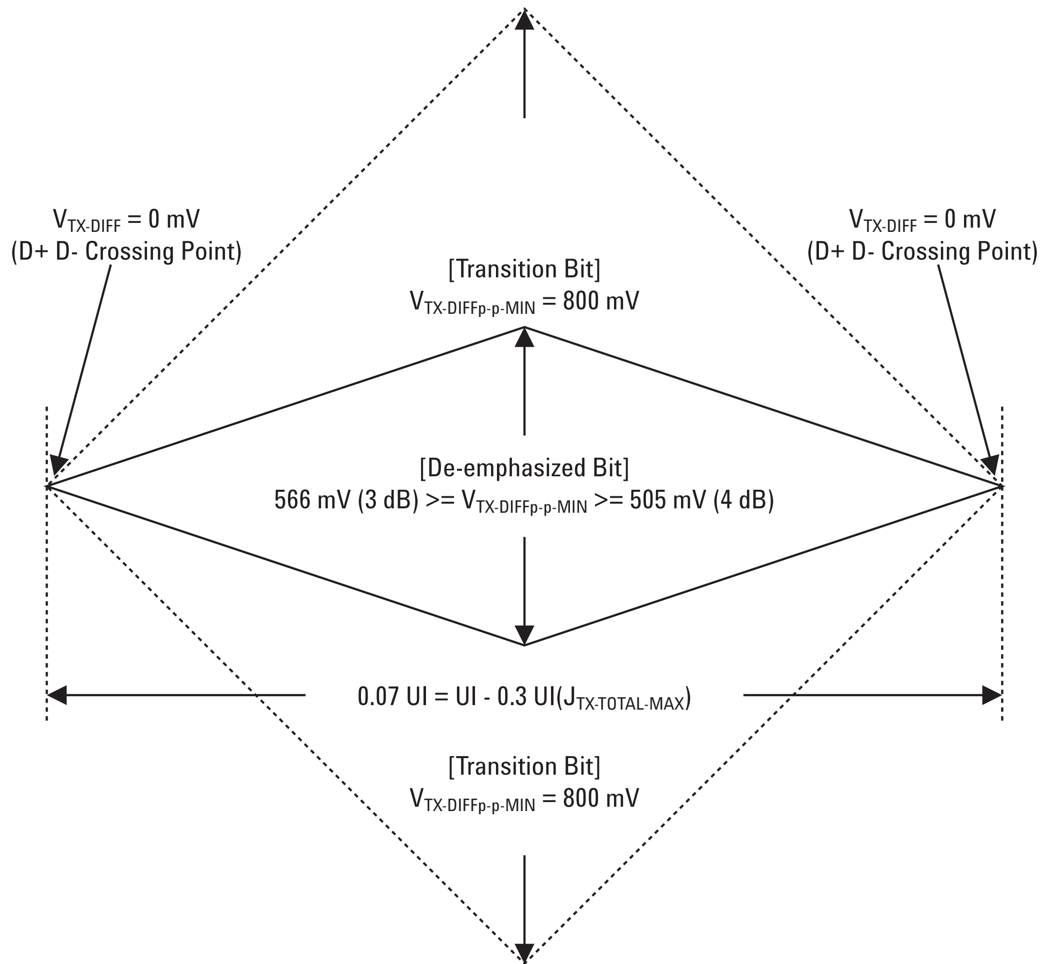


Figure 59 Minimum Transmitter Timing and Voltage Output Compliance Specification.

Test References

Table 4-9, PCI Express Base Specification v2.0.

Tx, Median to Max Jitter

Test Definition Notes from the Specification

Table 128 $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ from Table 4-5 of the Base Specification.

Symbol	Parameter	Min	Nom	Max
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.			0.125 UI

NOTE: Measured differently at zero crossing points after applying the 2.5 GT/s clock recovery function.

- Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to the recovered TX UI.
- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured using the clock recovery function specified in Section 4.3.3.2. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).

Limits

Maximum = 0.125 UI

Pass Condition

0.125 UI > $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$

Test Procedure

Follow the procedure in “Running Signal Quality Tests" on page 188, and select “Median to Max Jitter”.

Measurement Algorithm

A T_{TX-EYE} = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.25 UI for the Transmitter using the clock recovery function specified in Section 4.3.3.2 of the Base Specification. $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget using the clock recovery function specified in Section 4.3.3.2 of the Base Specification.

It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. This parameter is measured with the equivalent of a zero jitter reference clock. The T_{TX-EYE} measurement is to be met at the target bit error rate. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ is to be met using the compliance pattern at a sample size of 1,000,000 UI.

Test References

Table 4-9, PCI Express Base Specification v2.0.

Tx, Eye-Width

Test Definition Notes from the Specification

Table 129 Eye Width from Table 4-9 of the Base Specification: 2.5 and 5.0 GT/s Transmitter Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
T_{TX-EYE}	Transmitter Eye including all jitter sources	0.75 (min)	0.75 (min)	UI	Does not include SSC or Refclk jitter. Includes Rj at 10^{-12}. See below notes. Note that 2.5 GT/s and 5.0 GT/s use different jitter determination methods.

NOTE: Measurements at 5.0 GT/s require an oscilloscope with a bandwidth of ≥ 12.5 GHz, or equivalent, while measurements made at 2.5 GT/s require an oscilloscope with at least 6.2 GHz bandwidth. Measurement at 5.0 GT/s must de-convolve effects of compliance test board to yield an effective measurement at Tx pins. 2.5 GT/s may be measured within 200 mils of Tx device's pins, although de-convolution is recommended. At least 10^5 UI of data must be acquired.

NOTE 2: Transmitter jitter is measured by driving the Transmitter under tests with a low jitter "ideal" clock and connecting the DUT to a reference load.

NOTE 3: Transmitter raw jitter data must be convolved with a filtering function that represents the worst case CDR tracking BW. 2.5 GT/s and 5.0 GT/s use different filter functions. After the convolution process has been applied, the center of the resulting eye must be determined and used as a reference point for obtaining eye voltage and margins.

NOTE 4: For 5.0 GT/s, de-emphasis timing jitter must be removed. An Additional HPF function must be applied. This parameter is measured by accumulating a record length of 10^6 UI while the DUT outputs a compliance pattern. $T_{MIN-PULSE}$ is defined to be nominally 1 UI wide and is bordered on both sides by pulses of opposite polarity.

- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured using the clock recovery function specified in Section 4.3.3.2. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).

- A $T_{TX\text{-}EYE}$ = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX\text{-}JITTER\text{-}MAX}$ = 0.25 UI for the Transmitter using the clock recovery function specified in Section 4.3.3.2. $T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget using the clock recovery function specified in Section 4.3.3.2.

  It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. This parameter is measured with the equivalent of a zero jitter reference clock. The $T_{TX\text{-}EYE}$ measurement is to be met at the target bit error rate. The $T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ is to be met using the compliance pattern at a sample size of 1,000,000 UI.

Limits

Minimum = 0.75 UI

Pass Condition

0.75 UI < $T_{TX\text{-}EYE}$.

Test Procedure

Follow the procedure in “Running Signal Quality Tests" on page 188, and select “Eye-Width”.

Measurement Algorithm

The maximum Transmitter jitter can be derived as follows.

$$T_{\text{TX-MAX-JITTER}} = 1 - T_{\text{TX-EYE}} = 0.25\ \text{UI}$$

This parameter is measured with the equivalent of a zero jitter reference clock.

Test References

Table 4-9, PCI Express Base Specification v2.0.

Tx, Peak Differential Output Voltage

Test Definition Notes from the Specification

Table 130 Peak Differential Output Voltage from Table 4-9 of the Base Specification: 2.5 and 5.0 GT/s Transmitter Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$T_{TX\text{-}DIFF\text{-}PP}$	Differential p-p Tx voltage swing	0.8 (min) 1.2 (max)	0.8 (min) 1.2 (max)	V	As measured with compliance test load. Defined as 2*|V_{TXD+} - V_{TXD-}|.

- This is the ration of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition.
- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured using the clock recovery function specified in Section 4.3.3.2. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).

Test Procedure

Follow the procedure in “Running Signal Quality Tests" on page 188, and select “Peak Differential Output Voltage”.

Pass Condition

$0.8\ V \le V_{TX\text{-}DIFF\text{-}p\text{-}p} \le 1.2\ V$

Measurement Algorithm.

$$V_{\text{TX-DIFFp-p}} = 2 \times |V_{\text{TX-D+}} - V_{\text{TX-DIFF-}}|$$

Test References

Table 4-9, PCI Express Base Specification v2.0.

Tx, Rise/Fall Time

Test Definition Notes from the Specification

Table 131 Rise/Fall Time from Table 4-9 of the Base Specification: 2.5 and 5.0 GT/s Transmitter Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$T_{TX\text{-}RISE\text{-}FALL}$	Transmitter rise and fall time	0.125 (min)	0.15 (min)	UI	Measured differently from 20% to 80% of swing. See below Note.

NOTE: Measurements at 5.0 GT/s require an oscilloscope with a bandwidth of ≥ 12.5 GHz, or equivalent, while measurements made at 2.5 GT/s require a scope with at least 6.2 GHz bandwidth. Measurement at 5.0 GT/s must de-convolve effects of compliance test board to yield an effective measurement at Tx pins. 2.5 GT/s may be measured within 200 mils of Tx device's pins, although de-convolution is recommended. For measurement setup details, refer to below figure. At least 10^5 UI of data must be acquired.

Tx, Rise/Fall Time is defined in PCI Express Base Specification v2.0, Section 4.3.3.5 and Table 4-9.

- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 of the Base Specification and measured using the clock recovery function specified in Section 4.3.3.2. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 of the Base Specification.
- Measured between 20-80% at Transmitter package pins into a test load as shown in Figure 4-25 for both $V_{TX\text{-}D+}$ and $V_{TX\text{-}D-}$.

Limits

Minimum = 0.125 UI

Pass Condition

0.125 UI < $T_{TX\text{-}RISE}$, $T_{TX\text{-}FALL}$.

Test Procedure

Follow the procedure in "Running Signal Quality Tests" on page 188, and select "Rise/Fall Time".

Measurement Algorithms

Rise/Fall time is limited to only rising or falling edges of consecutive transitions for transmitter measurements. Rise/Fall Time is taken independently on each single ended waveform source when you use two single ended probes or two SMA cables as the signal source. Differential signal Rise/Fall Time show up when you select Differential probe type.

Rise Time. The Rise Time measurement is the time difference between when the VREF-HI reference level is crossed and the VREF-LO reference level is crossed on the rising edge of the waveform.

$t_{RISE}(n) = t_{HI+}(i) - t_{LO+}(j)$

Where:

t_{RISE} is a Rise Time measurement.

t_{HI+} is a set of t_{HI} for rising edges only.

t_{LO+} is a set of t_{LO} for rising edges only.

i and j are indexes for nearest adjacent pairs of t_{LO+} and t_{HI+}.

n is the index of rising edges in the waveform.

Rise Time for $v_{D+}(t)$ is as follows:

$t_{D+RISE}(n) = t_{D+HI+}(i) - t_{D+LO+}(j)$

and for $v_{D-}(t)$:

$t_{D-FALL}(n) = t_{D-LO-}(i) - t_{D-HI-}(j)$

Fall Time. The Fall Time measurement is the time difference between when the VREF-HI reference level is crossed and the VREF-LO reference level is crossed on the falling edge of the waveform.

$t_{FALL}(n) = t_{LO-}(i) - t_{HI-}(j)$

Where:

t_{FALL} is a Fall Time measurement.

t_{HI-} is set of t_{HI} for falling edge only.

t_{LO-} is set of t_{LO} for falling edge only.

i and j are indexes for nearest adjacent pairs of t_{LO-} and t_{HI-}.

n is the index of falling edges in the waveform.

Fall Time for $v_{D+}(t)$ is as follows:

$t_{D+FALL}(n) = t_{D+LO-}(i) - t_{D+HI-}(j)$

and for $v_{D-}(t)$:

$t_{D-FALL}(n) = t_{D-LO-}(i) - t_{D-HI-}(j)$

Test References

Table 4-9, PCI Express Base Specification v2.0.

Tx, De-emphasized Voltage Ratio

Test Definition Notes from the Specification

Table 132 De-emphasized Voltage Ratio from Table 4-9 of the Base Specification: 2.5 and 5.0 GT/s Transmitter Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$V_{TX\text{-}DE\text{-}RATIO\text{-}3.5dB}$	Tx de-emphasis level ratio	3.0 (min) 4.0 (max)	3.0 (min) 4.0 (max)	dB	See Section 4.3.3.9 and Note 11 for details.
$V_{TX\text{-}DE\text{-}RATIO\text{-}6dB}$	Tx de-emphasis level ratio	N/A	5.5 (min) 6.5 (max)	dB	See Section 4.3.3.9 and Note 11 for details.

NOTE: Root complex Tx de-emphasis is configured from Upstream controller. Downstream Tx de-emphasis is set via a command, issued at 2.5 GT/s. For details, refer to the appropriate location in Section 4.2.

Tx, De-emphasized Voltage Ratio is defined in PCI Express Base Specification v2.0, Section 4.3.3.5 and Table 4-9.

- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 of the Base Specification and measured using the clock recovery function specified in Section 4.3.3.2 of the Base Specification. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 of the Base Specification.

Limits

Minimum = -3.0 dB and Maximum = -4.0 dB

Pass Condition

$-4.0\ dB < V_{TX\text{-}DE\text{-}RATIO} < -3.0\ dB$.

Test Procedure

Follow the procedure in “Running Signal Quality Tests" on page 188, and select “De-emphasized Voltage Ratio”.

Measurement Algorithm

This is the ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.

Test References

Table 4-9, PCI Express Base Specification v2.0.

Running Common Mode Voltage Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 22. Then, when selecting tests, navigate to "Common Mode Voltage" in the "Transmitter (Tx) Tests" group.

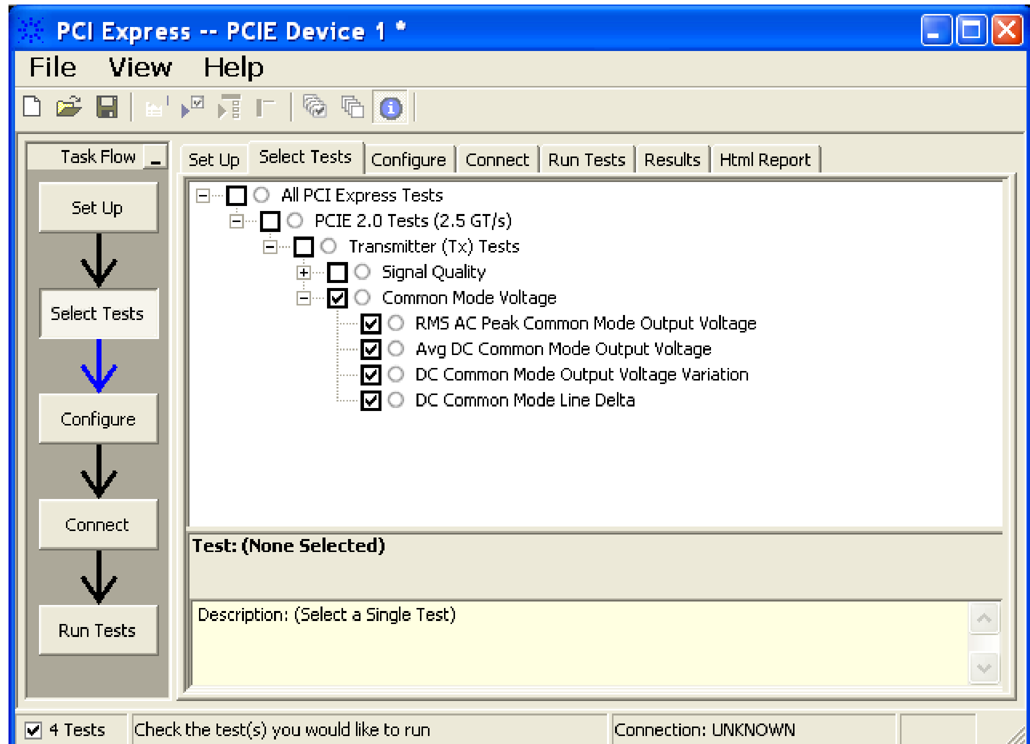


Figure 60 Selecting Transmitter (Tx) Common Mode Voltage Tests

Tx, RMS AC Peak Common Mode Output Voltage

Table 133 $V_{TX-CM-AC-P}$ from Table 4-9 of the Base Specification.

Symbol	Parameter	Min	Nom	Max
$V_{TX-CM-AC-P}$	RMS AC Peak Common Mode Output Voltage			20 mV

Test Definition Notes from the Specification

- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 of the Base Specification and measured using the clock recovery function specified in Section 4.3.3.2. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 of the Base Specification.

Limits

Maximum = 20 mV

Pass Condition

20 mV > $V_{TX-CM-ACp}$.

Test Procedure

Follow the procedure in “Running Common Mode Voltage Tests" on page 201, and select “RMS AC Peak Common Mode Output Voltage”.

NOTE This test is only available when the single-ended or SMA probing method has been used (see “Probing the Link for Tx Compliance" on page 184).

Measurement Algorithm

$$V_{\text{TX-CM-ACp}} = RMS\left(\frac{|V_{\text{TX-D+}} + V_{\text{TX-D-}}|}{2} - V_{\text{TX-CM-DC}}\right)$$

$$V_{\text{TX-CM-DC}} = DC_{(avg)} \text{ of } \frac{|V_{\text{TX-D+}} + V_{\text{TX-DC-}}|}{2}$$

Test References

Table 4-9, PCI Express Base Specification v2.0.

Tx, Avg DC Common Mode Output Voltage

Test Definition Notes from the Specification

Table 134 Average DC Common Mode Output Voltage from Table 4-9 of the Base Specification: 2.5 and 5.0 GT/s Transmitter Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$V_{TX-DC-CM}$	Transmitter DC common-mode voltage	0 (min) 3.6(max)	0 (min) 3.6 (max)	V	The allowed DC common-mode voltage at the Transmitter pins under any conditions.

Tx, Average DC Common Mode Output Voltage is defined in PCI Express Base Specification v2.0, Section 4.3.3.5 and Table 4-9.

- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured using the clock recovery function specified in Section 4.3.3.2. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).

Limits

$0 \text{ V} \leq V_{TX-DC-CM} \leq 3.6 \text{ V}$

Test Procedure

Follow the procedure in “Running Common Mode Voltage Tests" on page 201, and select “Avg DC Common Mode Output Voltage”.

NOTE

This test is only available when the single-ended or SMA probing method has been used (see “Probing the Link for Tx Compliance" on page 184).

Measurement Algorithm

The Avg DC Common Mode Voltage measurement computes the DC average of the common mode signal:

$$V_{\text{TX-CM-DC}} = DC_{(avg)} \text{ of } \frac{|V_{\text{TX-D+}} + V_{\text{TX-DC-}}|}{2}$$

NOTE

The base specification states that $V_{TX-DC-CM}$ must be held at the same value during all states. For complete validation, this measurement should be performed on the device in all states and the results compared.

Test References

Table 4-9, PCI Express Base Specification v2.0.

Tx, DC Common Mode Line Delta

Test Definition Notes from the Specification

Table 135 DC Common Mode Line Delta from Table 4-9 of the Base Specification: 2.5 and 5.0 GT/s Transmitter Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0 (min) 25(max)	0 (min) 25 (max)	mV	$\lvert V_{TX\text{-}CM\text{-}DC\text{-}D+[during\ L0]} - V_{TX\text{-}CM\text{-}DC\text{-}D\text{-}[during\ L0]} \rvert \leq$ 25mV $V_{TX\text{-}CM\text{-}DC\text{-}D}$ - $DC_{(avg)}$ of $\lvert V_{TX\text{-}D+} \rvert$ [during L0] $V_{TX\text{-}CM\text{-}DC\text{-}D}$ - $DC_{(avg)}$ of $\lvert V_{TX\text{-}D\text{-}} \rvert$ [during L0]

Tx, DC Common Mode Line Delta is defined in PCI Express Base Specification v2.0, Section 4.3.3.5 and Table 4-9.

- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured using the clock recovery function specified in Section 4.3.3.2. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).

Limits

$0\ V < V_{TX\text{-}CM\text{-}LINE\text{-}DELTA} \leq 25mV$

Test Procedure

Follow the procedure in “Running Common Mode Voltage Tests" on page 201, and select “DC Common Mode Line Delta”.

NOTE

This test is only available when the single-ended or SMA probing method has been used (see “Probing the Link for Tx Compliance" on page 184).

Measurement Algorithm

$$\left|V_{\text{TX-CM-DC-D+}} - V_{\text{TX-DM-DC-D-}}\right| \leq 25 \text{ mV}$$

$$V_{\text{TX-CD-DC-D+}} = DC_{(avg)} \text{ of } \left|V_{\text{TX-D+}}\right|$$

$$V_{\text{TX-CD-DC-}} = DC_{(avg)} \text{ of } \left|V_{\text{TX-D-}}\right|$$

Test References

Table 4-9, PCI Express Base Specification v2.0.

Tx, DC Common Mode Output Voltage Variation

Test Definition Notes from the Specification

The TX DC common mode voltage ($V_{TX-DC-CM}$) must be held at the same value during all states. The allowable range for $V_{TX-DC-CM}$ is 0 to 3.6 V (±100 mV).

Limits

$|V_{TX-DC-CM-VARIATION}| \leq 100$ mV

Test Procedure

Follow the procedure in "Running Common Mode Voltage Tests" on page 201, and select "DC Common Mode Output Voltage Variation".

NOTE This test is only available when the single-ended or SMA probing method has been used (see "Probing the Link for Tx Compliance" on page 184).

Measurement Algorithm

The Tx DC Common Mode Output Voltage Variation measurement computes the worst case positive or negative excursion of the common mode signal from the average DC Common Mode Voltage $V_{TX-DC-CM}$

$$V_{TX-DC-CM-VARIATION} = |\ \text{Max}(\text{Max}(V_{CM(i)}), \text{Min}(V_{CM(i)})) - V_{TX-DC-CM}\ |$$

Where:

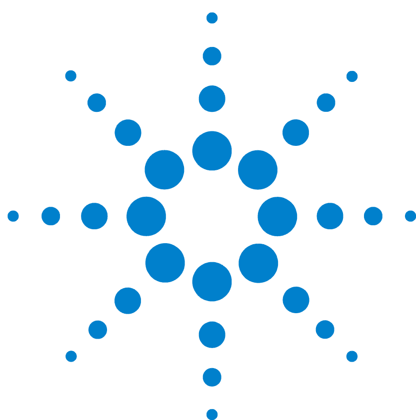
i is the index of all waveform values.

V_{CM} is the common mode signal $(V_{TX-D+} + V_{TX-D-})/2$.

Test References

Table 136 DC Common Mode Output Voltage Variation Test References

Test Name	Reference	PCI-SIG Assertions
DC Common Mode Output Voltage Variation	PHY ELECTRICAL TEST CONSIDERATIONS, REVISION 1.0RD, Section 4.1.6	PHY.3.1#12



12 Transmitter (Tx) Tests, 2.5 GT/s, PCI-E 2.0, Low Power

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Tx Compliance Test Load 209
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Running Common Mode Voltage Tests 212

This section provides the Methods of Implementation (MOIs) for Transmitter tests using an Agilent 54855A, 80000B, or 90000A series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

The PCIe 2.0 base specification describes the Low Power specification as optional. From “4.3.3.2. Low and Full Swing Transmitter Output Levels”:

> Both the 2.5 GT/s and 5.0 GT/s PCI Express specifications define two voltage swing levels: full swing and low swing. Full swing signaling implements de-emphasis, while low swing does not. Typically, low swing is specified for power sensitive applications where a shorter channel is acceptable. The requirement as to whether a Transmitter need support full swing, low swing, or both modes, is dependent on its usage model. The method by which the output mode is selected is not explicitly defined in this specification, and may be implementation dependent. Note: All PCI Express device Transmitters must support full swing signaling, while support for half swing signaling is optional.
>
> While two different Transmitter output signaling levels are defined, only a single Receiver specification is defined; this implies that margins (as specified at the Receiver) are identical regardless of the Transmitter's output swing capabilities. It also implies that the channel’s characteristics need to be matched to the Transmitter output swing. Typically, low swing output is utilized for short channels, such as would occur in mobile platforms.

PCIe 2.0 Low Power Transmitter Tests consist of all tests from PCIe 2.0 Full (Standard) Power Tests except de-emphasis Tests. The following table shows all the PCIe 2.0 Low Power Tests:

Table 137 PCIE 2.0 Low Power Transmitter Tests

Test Name	Remarks	See
Unit Interval	Same as Full Power	page 190.
Template Tests	Different	page 210.
Median to Max Jitter	Different	page 210.
Eye-Width	Different	page 210.
Peak Differential Output Voltage	Different	page 211.
Rise/Fall Time	Same as Full Power	page 197.
RMS AC Peak Common Mode Output Voltage	Same as Full Power	page 202.
Avg DC Common Mode Output Voltage	Same as Full Power	page 203.
DC Common Mode Output Voltage Variation	Same as Full Power	page 205.
DC Common Mode Line Delta	Same as Full Power	page 204.

All the tests above remarked with “Same as Full Power” share the same Method of Implementation (MOI) with PCIE 2.0 Full Power (refer to the page numbers shown). The differences in the test method are described in this chapter.

Probing the Link for Tx Compliance

When performing low-power transmitter tests, probing is the same as for full-power tests. See “Probing the Link for Tx Compliance" on page 184.

Tx Compliance Test Load

When performing low-power transmitter tests, the compliance test load is the same as for full-power tests. See “Tx Compliance Test Load" on page 188.

Running Signal Quality Tests

Start the automated testing application as described in “Starting the PCI Express Automated Test Application" on page 22. Then, when selecting tests, navigate to “Signal Quality” in the “Transmitter (Tx) Tests” group.

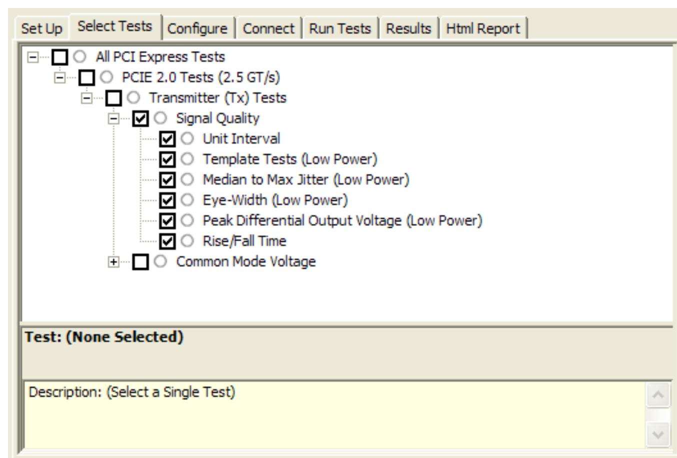


Figure 61 Selecting Transmitter (Tx) Signal Quality Tests

Tx, Unit Interval

When performing low-power transmitter tests, the Tx Unit Interval test is the same as for full-power tests. See “Tx, Unit Interval" on page 190.

Tx, Template Tests (Low Power)

Test Definition/Reference

PCIE base specification 2.0 section 4.3.3.5.

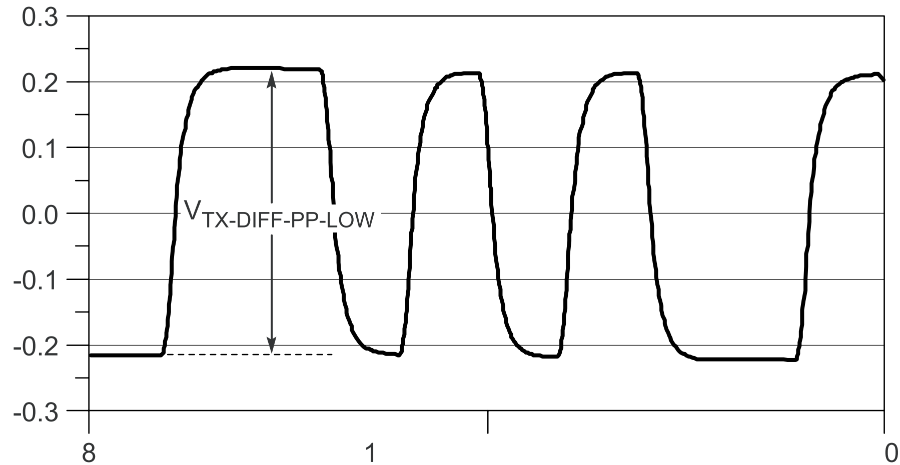


Figure 62 Low Swing Tx Parameters, Figure 4-27 in Base Specification v2.0

Difference in Test Procedure Compared to Full Power

- Different Eye diagram used. The Eye diagram can be found in Figure 2.2 of Mobile Low Power PCIE Specification.
- Eye diagram only runs once with both transition and non-transition bits since de-emphasis is no longer needed for low power specification.

See Also "Tx, Template Tests" on page 191.

Tx, Median to Max Jitter (Low Power)

Difference in Test Procedure Compared to Full Power

- Eye diagram only runs once with both transition and non-transition bits since de-emphasis is no longer needed for low power specification.

See Also "Tx, Median to Max Jitter" on page 192.

Tx, Eye-Width (Low Power)

Difference in Test Procedure Compared to Full Power

- Eye diagram only runs once with both transition and non-transition bits since de-emphasis is no longer needed for low power specification.

See Also "Tx, Eye-Width" on page 194.

Tx, Peak Differential Output Voltage (Low Power)

Difference in Test Procedure Compared to Full Power

- Different specification used:

Table 138 Peak Differential Output Voltage from Table 4-9 of the Base Specification: 2.5 and 5.0 GT/s Transmitter Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$T_{TX-DIFF-PP-LOW}$	Low power differential p-p Tx voltage swing	0.4 (min) 1.2 (max)	0.4 (min) 1.2 (max)	V	As measured with compliance test load. Defined as $2^* \| V_{TXD+} - V_{TXD-} \|$.

- Low swing output, defined by VTX-DIFF-PP-LOW must be implemented as shown in Figure 4-27 (Base Specification) with no de-emphasis.

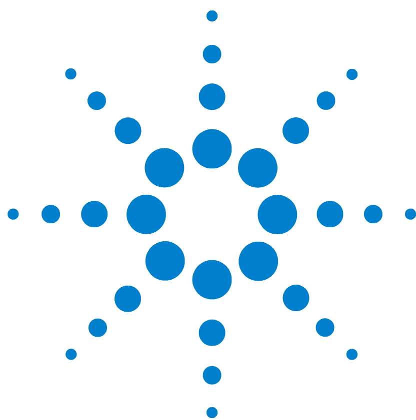
See Also "Tx, Peak Differential Output Voltage" on page 196.

Tx, Rise/Fall Time

When performing low-power transmitter tests, the Tx Rise/Fall Time test is the same as for full-power tests. See "Tx, Rise/Fall Time" on page 197.

Running Common Mode Voltage Tests

When performing low-power transmitter tests, the common mode voltage tests are the same as for full-power tests. See "Running Common Mode Voltage Tests" on page 201.



13
Receiver (Rx) Tests, 2.5 GT/s, PCI-E 2.0

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Running Receiver Tests 217

This section provides the Methods of Implementation (MOIs) for Receiver tests using an Agilent 54855A, 80000B, or 90000A series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

NOTE None of the included receiver tests validate the receiver's ability to correctly receive data (also known as receiver tolerance). Rather, they validate that the signal as seen by the receiver meets or exceeds various parameters (maximum voltage, jitter, eye width, etc.). These tests validate the transmitter and interconnect. Separate receiver tolerance testing is required to ensure the receiver is correctly receiving data.

Probing the Link for Rx Compliance

Receiver tests are done by probing the link as close as is feasibly possible to the pins of the receiver device. Alternatively, a dummy load can be used for the termination of the link. To probe the receiver link, you can:

- Use two differential probe heads with two 1134A probe amplifiers (with the negative lead grounded for single-ended measurements) and the channel 1 and channel 3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.
- Use one differential probe head with the 1134A probe amplifier and the channel 2 input of an oscilloscope that has 20 GS/s sample rate available on that channel.

Table 139 Probing Options for Receiver Testing

	Probing Configurations			**Captured Waveforms**		**System Specifications**	
						54855A	
	Probing Method	**Break Serial Link**	**Channels Used**	**Differential Mode**	**Common Mode**	**System Band Width**	**Rise* Time (20-80)**
DUT Connection	Single-Ended (2 x 1134A w/ Differential Probe Heads)	Y/N	2	Pseudo	Yes	6 GHz	70 ps
	Differential (1 x 1134A w/ Differential Probe Head)	Y/N	1	True	No	6 GHz	70 ps

*Typical

Single-Ended Probing

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Source 1 - Source 2. The Sources can be either channels 1 and 3 or channels 2 and 4. The Common mode measurements are also available in this configuration from the common mode waveform (Source 1 + Source 2)/2.

Make sure to probe equal distances from the receiver, as close as possible to the receiver, with the shortest ground connection possible.

This probing technique can be used for either a live link that is transmitting data, or a link terminated into a “dummy load.”

Channel-to-channel deskew is required using this technique because two channels are used.

For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 392.

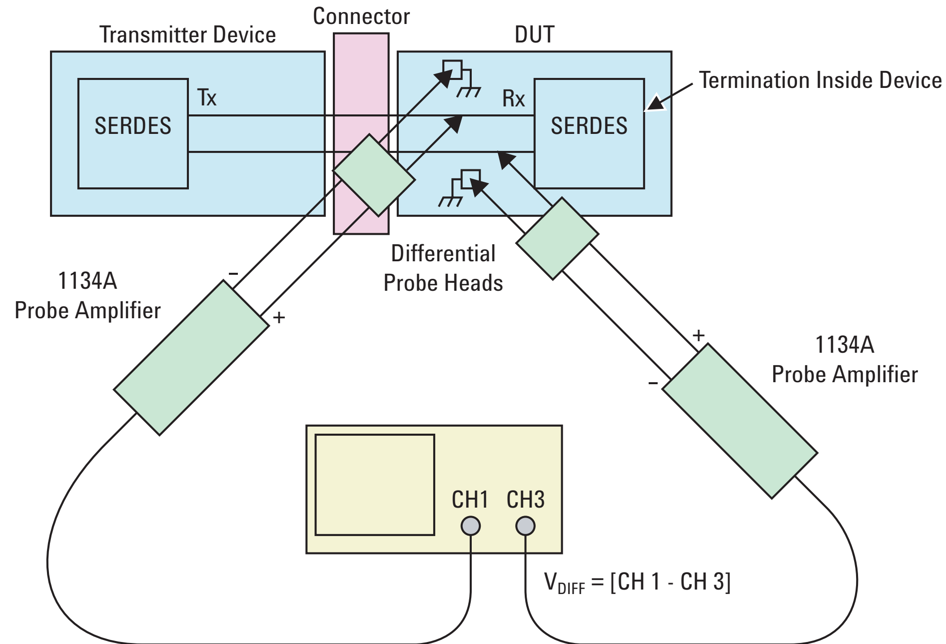


Figure 63 Single-Ended Probing

Differential Probing

The differential signal is measured directly by the differential probe head.

Make sure to probe equal distances from the receiver, as close as possible to the receiver, with the shortest ground connection possible.

This probing technique can be used for either a live link that is transmitting data, or a link terminated into a “dummy load.”

A single channel of the oscilloscope is used, so de-skew is not necessary.

For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 392.

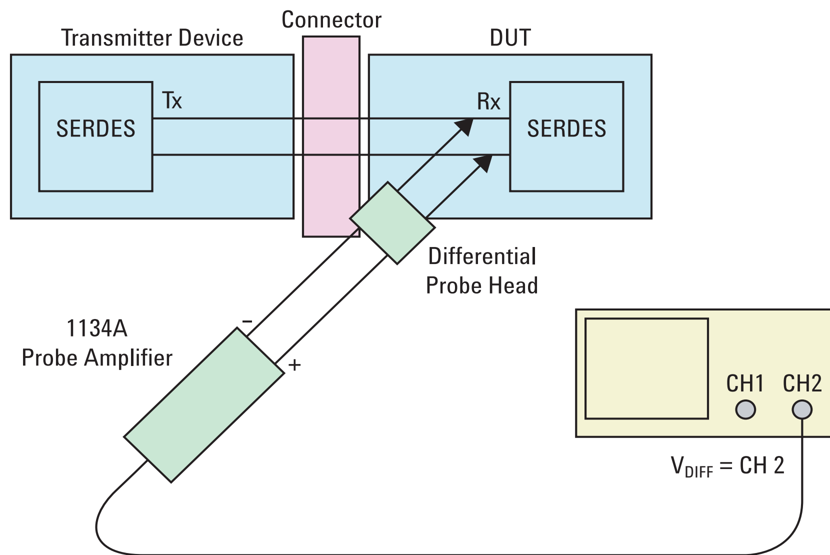


Figure 64 Differential Probing

Running Receiver Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 22. Then, when selecting tests, navigate to the "Receiver (Rx) Tests" group.

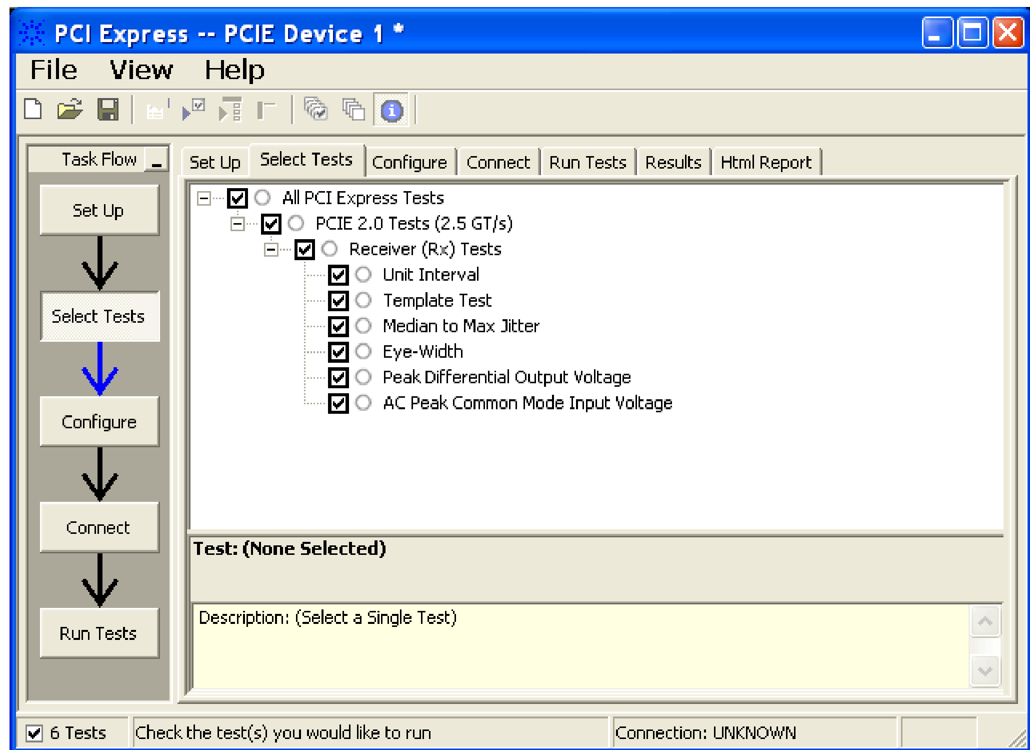


Figure 65 Selecting Receiver (Rx) Tests

Rx, Unit Interval

Test Definition Notes from the Specification

Table 140 Unit Interval from Table 4-12 of the Base Specification: 2.5 and 5.0 GT/s Receiver Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
UI	Unit Interval	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)	ps	UI does not account for SSC caused variations.

Test References

Table 4-12, PCI Express Base Specification v2.0.

Test Definition Notes from the Specification

- UI (Unit Interval) is specified to be ±300 ppm.
- UI does not account for SSC dictated variations.
- No test load is necessarily associated with this value.

Rx, Template Test

See Section 4.3.4 of the Base Specification for additional notes and test definitions.

Test Definition Notes from the Specification

- The RX eye diagram in Figure 4-26 of the Base Specification is specified using the passive compliance/test measurement load (see Figure 4-25, Base Specification) in place of any real PCI Express RX component.

NOTE

In general, the minimum Receiver eye diagram measured with the compliance/test measurement load (see Figure 4-25, Base Specification) will be larger than the minimum Receiver eye diagram measured over a range of systems at the input Receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input Receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 4-26, Base Specification) expected at the input Receiver based on some adequate combination of system simulations and the Return Loss measured looking into the RX package and silicon.

- The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.
- The eye diagram must be valid for any 250 consecutive UIs.
- A recovered RX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the RX UI.

Test Procedure

Follow the procedure in "Running Receiver Tests" on page 217, and select "Template Test".

Test References

Table 4-12, PCI Express Base Specification v2.0.

The total number of mask violation shall be 0.

Rx, Median to Max Jitter

Table 141 $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ from Table 4-12 of the Base Specification

Symbol	Parameter	Min	Nom	Max
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time delta between the jitter median and maximum deviation from the median.			0.3 UI

Test Definition Notes from the Specification

- Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to the recovered TX UI to be measured after the clock recovery function in Section 4.3.3.2.
- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured using the clock recovery function specified in Section 4.3.3.2. Also refer to the Transmitter compliance eye diagram shown in Figure 4-26 (Base Specification). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered using the clock recovery function specified in Section 4.3.3.2 must be used as a reference for the eye diagram.
- The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total 0.64. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. The RX UI recovered using the clock recovery function specified in Section 4.3.3.2 must be used as the reference for the eye diagram. The T_{RX-EYE} measurement is to be met at the target bit error rate. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ is to be met using the compliance pattern at a sample size of 1,000,000 UI.

Limits

Maximum = 0.3 UI

Pass Condition

0.3 UI > $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$.

Test Procedure

Follow the procedure in "Running Receiver Tests" on page 217, and select "Median to Max Jitter".

Measurement Algorithm

Refer to "Rx, Median to Max Jitter" on page 219 for Rx Median-to-Max Jitter measurement algorithm.

Test References

Table 4-12, PCI Express Base Specification v2.0.

Rx, Eye-Width

Table 142 T_{RX-EYE} from Table 4-12 of the Base Specification

Symbol	Parameter	Min	Nom	Max
T_{RX-EYE}	Minimum Receiver Eye Width	0.4 UI		

Test Definition Notes from the Base Specification

- The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI.
- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured using the clock recovery function specified in Section 4.3.3.2. Also refer to the Transmitter compliance eye diagram shown in Figure 4-26 (Base Specification). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered using the clock recovery function specified in Section 4.3.3.2 must be used as a reference for the eye diagram.

- The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total 0.64. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. The RX UI recovered using the clock recovery function specified in Section 4.3.3.2 must be used as the reference for the eye diagram. The T_{RX-EYE} measurement is to be met at the target bit error rate. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ is to be met using the compliance pattern at a sample size of 1,000,000 UI.
- See the “PCI Express Jitter and BER” white paper for more details on the Rx-Eye measurement.

Limits

Minimum = 0.40 UI

Pass Condition

0.40UI < T_{RX-EYE}.

Test Procedure

Follow the procedure in “Running Receiver Tests" on page 217, and select “Eye-Width”.

Measurement Algorithm

Refer to “Rx, Eye-Width" on page 220 for Eye Width measurement algorithm.

Test References

Table 4-12, PCI Express Base Specification v2.0.

Rx, Peak Differential Output Voltage

Test Definition Notes from the Specification

Table 143 Peak Differential Output Voltage from Table 4-12 of the Base Specification: 2.5 and 5.0 GT/s Receiver Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$V_{RX\text{-}DIFF\text{-}PP\text{-}CC}$	Differential Rx peak-peak voltage for common Refclk Rx architecture	0.175 (min) 1.2 (max)	0.120 (min) 1.2 (max)	V	See Section 4.3.7.2.2.
$V_{RX\text{-}DIFF\text{-}PP\text{-}DC}$	Differential Rx peak-peak voltage for data clocked Rx architecture	0.175 (min) 1.2 (max)	0.100 (min) 1.2 (max)	V	See Section 4.3.7.2.2.

- $V_{RX\text{-}DIFFp\text{-}p} = 2^*|V_{RX\text{-}D+} - V_{RX\text{-}D-}|$
- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured using the clock recovery function specified in Section 4.3.3.2. Also refer to the Transmitter compliance eye diagram shown in Figure 4-26 (Base Specification). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered using the clock recovery function specified in Section 4.3.3.2 must be used as a reference for the eye diagram.

Test Procedure

Follow the procedure in “Running Receiver Tests" on page 217, and select “Peak Differential Output Voltage”.

Limits

Minimum = 0.40 UI and Maximum = 1.200 V

Pass Condition

$0.175 \text{ V} < V_{RX\text{-}DIFFp\text{-}p} < 1.200 \text{ V}$

Measurement Algorithm

Refer to “Rx, Peak Differential Output Voltage" on page 222 for Differential Voltage measurement algorithms.

NOTE

For receiver testing, Eye Height is measured on all UIs.

Test References

Table 4-12, PCI Express Base Specification v2.0.

Rx, AC Peak Common Mode Input Voltage

Table 144 $V_{RX-CM-AC-P}$ from Table 4-12 of the Base Specification

Symbol	Parameter	Min	Nom	Max
$V_{RX-CM-AC-P}$	AC Peak Common Mode Input Voltage			150 mV

Test Definition Notes from Specification

- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured using the clock recovery function specified in Section 4.3.3.2. Also refer to the Transmitter compliance eye diagram shown in Figure 4-26 (Base Specification). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered using the clock recovery function specified in Section 4.3.3.2 must be used as a reference for the eye diagram.

Limits

Maximum = 150 mV

Pass Condition

150 mV > $V_{RX-CM-ACp}$.

Test Procedure

Follow the procedure in “Running Receiver Tests" on page 217, and select “AC Peak Common Mode Input Voltage”.

Measurement Algorithms

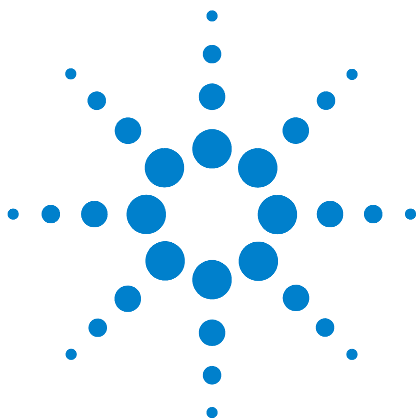
This measurement is made over 250 consecutive bits defined in Section 3.4 of the Base Specification.

$$V_{\text{RX-CM-AC}} = \frac{|V_{\text{RX-D+}} + V_{\text{RX-D-}}|}{2} - V_{\text{RX-CM-DC}}$$

$$V_{\text{RX-CM-DC}} = DC_{(avg)} \text{ of } \frac{|V_{\text{RX-D+}} + V_{\text{RX-D-}}|}{2}$$

Test References

Table 4-12, PCI Express Base Specification v2.0.



14
Add-In Card (Tx) Tests, 2.5 GT/s, PCI-E 2.0

Probing the Link for Add-In Card Compliance 226
Running Add-In Card Tests 229

This section provides the Methods of Implementation (MOIs) for Add-In Card Transmitter tests using an Agilent 54855A, 80000B, or 90000A series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

Probing the Link for Add-In Card Compliance

Connecting the Signal Quality Load Board for Add-in Card Testing

There are multiple pairs of SMA connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1 With the Add-in card fixture power supply powered off, connect the power supply connector to the Add-in card test fixture, and connect the device under test add-in card to the by-16 or by-1 connector slot.

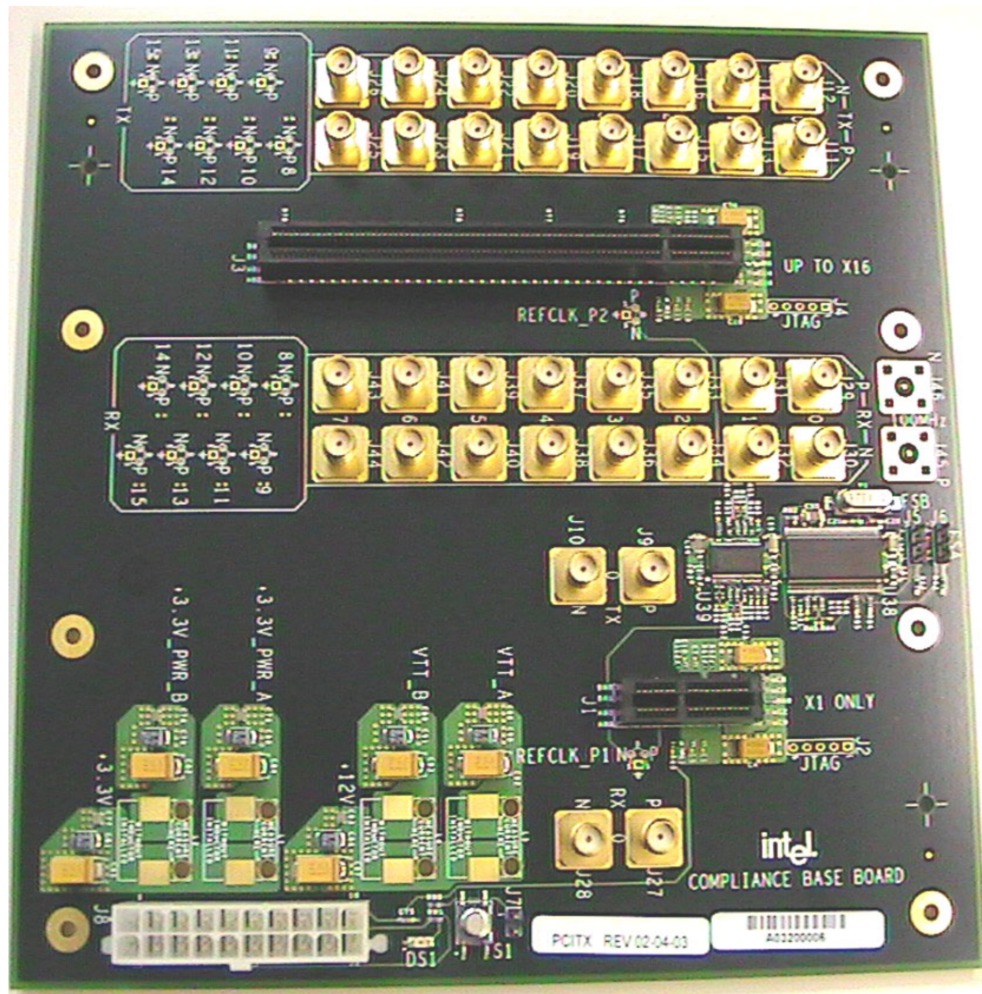


Figure 66 Compliance Base Board (CBB) Add-in Card Fixture

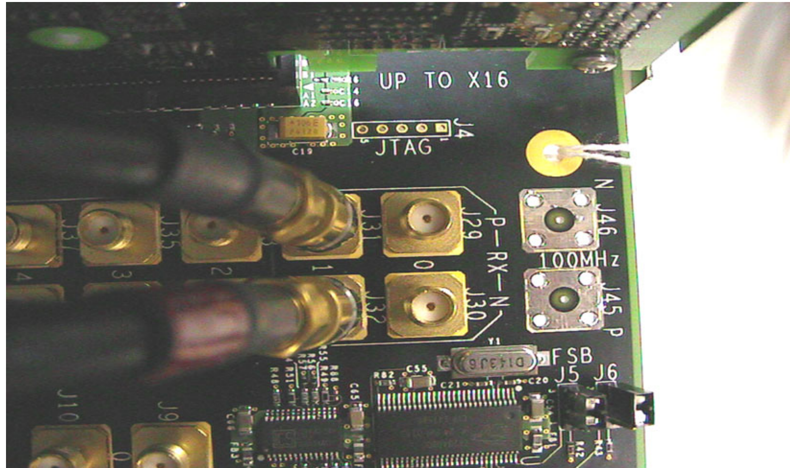


Figure 67 Compliance Base Board (CBB) SMA Probing Option

2 Connect cables up as follows:

   a Digital Storage Oscilloscope channel 1 to the TX LANE P under test (where Lane 1 is under test in this example shown in Figure 67 above).

   b Digital Storage Oscilloscope channel 3 to the TX LANE N under test (where Lane 1 is under test in this example shown in Figure 67 above).

NOTE The Compliance Base Board labeled PCITX Rev 02-04-03 silk screen incorrectly labels the add-in card transmitter probing locations as RX.

When SMA probing and two channels are used, channel-to-channel deskew is required (see “Channel-to-Channel De-skew" on page 386).

Not all lanes have SMA probing options. For signal quality testing of the remaining lanes you will need to use a high bandwidth differential or single ended probes (see Figure 68 on page 228). For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 392.

When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the 1134A probe amplifier.

When using a single differential probe head, use oscilloscope channel 2.

3 Connect adequate load to the power supply to assure it is regulating and turned on. Generally, one IDE hard drive will provide adequate load.

4 Turn on the power supply. DS1 LED (located near the ATX power supply connector) should turn on. If the LED is on, but the power supply does not turn on, check that the jumper J7 is installed between J7-1 and J7-2.

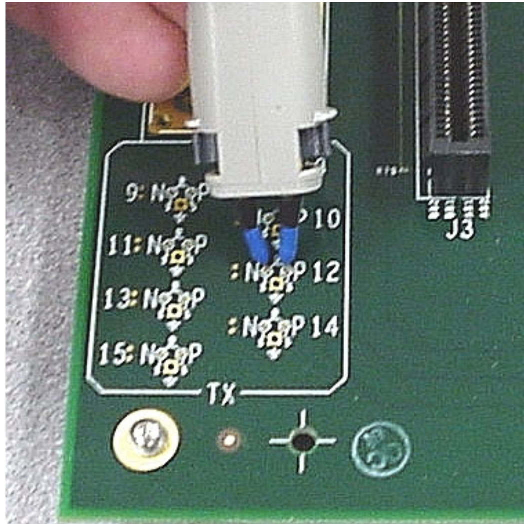


Figure 68 Compliance Base Board (CBB) Active Probing Option

Running Add-In Card Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 22. Then, when selecting tests, navigate to the "Add-In Card (Tx) Tests" group.

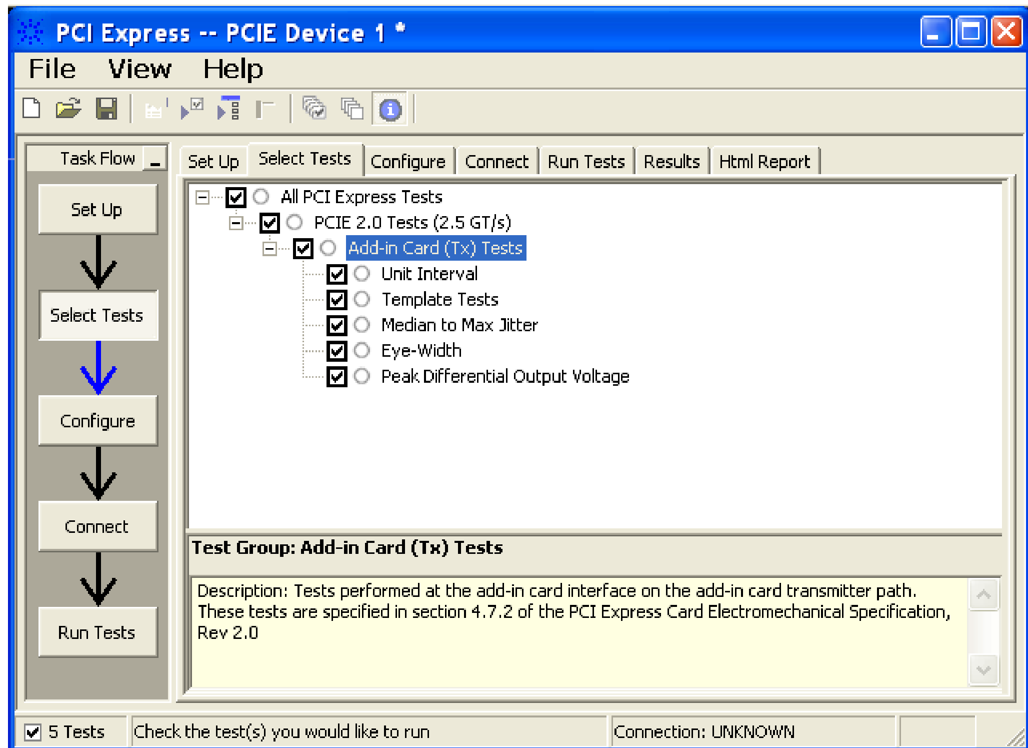


Figure 69 Selecting Add-In Card (Tx) Tests

Add-In Card Tx, Unit Interval

Test Definition Notes from the Specification

Table 145 Unit Interval from Table 4-9 of the Base Specification: 2.5 and 5.0 GT/s Transmitter Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
UI	Unit Interval	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)	ps	The specified UI is equivalent to a tolerance of ±300 ppm for each Refclk source. Period does not account for SSC caused variations. See below note.

NOTE: SSC permits a +0, -5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33 kHz.

- UI (Unit Interval) is specified to be ±300 ppm.
- UI does not account for SSC dictated variations.

Test Procedure

Follow the procedure in "Running Add-In Card Tests" on page 229, and select "Unit Interval".

Pass Condition

399.88ps ≤ UI ≤ 400.12ps

Measurement Algorithm

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window.

TX UI(p) = Mean(UI(n))

Where:

n is the index of UI in the clock recovery window.

p indicates the pth 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI, as described below.

NOTE The UI measurement is not required at this point. It is provided as an informative test only.

NOTE

The TX UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another TX UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case TX UI is reported.

Test References

Table 4-9, Section 4.3.3.5, PCI Express Base Specification v2.0.

Add-In Card Tx, Template Tests

Test Definition Notes from the Specification

Table 146 Add-in Card Transmitter Path Compliance Eye Requirements from Table 4-7 of the Base Specification at 2.5 GT/s

Parameter	Min	Max	Unit	Comments
V_{TXA}	360	1200	mV	Notes 1, 2, 5
V_{TXA_d}	514	1200	mV	Notes 1, 2, 5

NOTES 1: An ideal reference clock without jitter is assumed for this specification. All links are assumed active while generating this eye diagram.

NOTES 2: Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.

NOTES 3: T_{TXA} is the minimum eye width. The sample size for this measurement is 10^6 UI. This value can be reduced to 274 ps for simulation purpose at BER 10^{-12}.

NOTE 4: $J_{TXA-MDEDIAN-to-MAX-JITTER}$ is the maximum median-to-peak jitter outlier as defined in the “PCI Express Base Specification, Revision 1.1.” The sample size for this measurement is 10^6 UI. This value can be increased to 63 ps for simulation purposes at a BER of 10^{-12}.

NOTES 5: The values in Table 146 are referenced to an ideal 100 Ω differential load at the end of an isolated 3-inch long 85 Ω differential trace behind a standard PCI Express connector. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PHY Electrical Test Considerations for PCI Express Architecture* document.

Test References

Table 4-7, Section 4.7.1, PCI Express Base Specification v2.0.

Add-In Card Tx, Median to Max Jitter

Test Definition Notes from the Specification

Table 147 Add-in Card Transmitter Path Compliance Eye Requirements from Table 4-7 of the Base Specification at 2.5 GT/s

Parameter	Min	Max	Unit	Comments
T_{TXA}	287		ps	Notes 1, 3, 5
$J_{TXA\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	126	56.5	ps	Notes 1, 4, 5

NOTES 1: An ideal reference clock without jitter is assumed for this specification. All links are assumed active while generating this eye diagram.

NOTES 2: Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.

NOTES 3: T_{TXA} is the minimum eye width. The sample size for this measurement is 10^6 UI. This value can be reduced to 274 ps for simulation purpose at BER 10^{-12}.

NOTE 4: $J_{TXA\text{-}MDEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ is the maximum median-to-peak jitter outlier as defined in the “PCI Express Base Specification, Revision 1.1.” The sample size for this measurement is 10^6 UI. This value can be increased to 63 ps for simulation purposes at a BER of 10^{-12}.

- NOTES 5: The values in Table 147 are referenced to an ideal 100 Ω differential load at the end of an isolated 3-inch long 85 Ω differential trace behind a standard PCI Express connector. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PHY Electrical Test Considerations for PCI Express Architecture* document.

Limits

Maximum = 56.5 ps

Pass Condition

56.5 ps ≤ $T_{TXA\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$

Test Procedure

Follow the procedure in “Running Add-In Card Tests" on page 229, and select “Median to Max Jitter”.

Test References

Table 4-7, Section 4.7.1, PCI Express Base Specification v2.0.

Add-In Card Tx, Eye-Width

Test Definition Notes from the Specification

Table 148 Add-in Card Transmitter Path Compliance Eye Requirements from Table 4-7 of the Base Specification at 2.5 GT/s

Parameter	Min	Max	Unit	Comments
T_{TXA}	287		ps	Notes 1, 3, 5
$J_{TXA\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	126	56.5	ps	Notes 1, 4, 5

NOTES 1: An ideal reference clock without jitter is assumed for this specification. All links are assumed active while generating this eye diagram.

NOTES 2: Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.

NOTES 3: T_{TXA} is the minimum eye width. The sample size for this measurement is 10^6 UI. This value can be reduced to 274 ps for simulation purpose at BER 10^{-12}.

NOTE 4: $J_{TXA\text{-}MDEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ is the maximum median-to-peak jitter outlier as defined in the “PCI Express Base Specification, Revision 1.1.” The sample size for this measurement is 10^6 UI. This value can be increased to 63 ps for simulation purposes at a BER of 10^{-12}.

- NOTES 5: The values in Table 148 are referenced to an ideal 100 Ω differential load at the end of an isolated 3-inch long 85 Ω differential trace behind a standard PCI Express connector. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PHY Electrical Test Considerations for PCI Express Architecture* document.

NOTE

The median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

Limits

Minimum = 287 ps

Pass Condition

287 ps ≤ T_{TXA}

Test Procedure

Follow the procedure in “Running Add-In Card Tests" on page 229, and select “Eye-Width”.

Test References

Table 4-7, Section 4.7.1, PCI Express Base Specification v2.0.

Add-In Card Tx, Peak Differential Output Voltage

Test Definition Notes from the Specification

Table 149 Add-in Card Transmitter Path Compliance Eye Requirements from Table 4-7 of the Base Specification at 2.5 GT/s

Parameter	Min	Max	Unit	Comments
V_{TXA}	360	1200	mV	Notes 1, 2, 5
V_{TXA_d}	514	1200	mV	Notes 1, 2, 5

NOTES 1: An ideal reference clock without jitter is assumed for this specification. All links are assumed active while generating this eye diagram.

NOTES 2: Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.

NOTES 3: T_{TXA} is the minimum eye width. The sample size for this measurement is 10^6 UI. This value can be reduced to 274 ps for simulation purpose at BER 10^{-12}.

NOTE 4: $J_{TXA-MDEDIAN-to-MAX-JITTER}$ is the maximum median-to-peak jitter outlier as defined in the “PCI Express Base Specification, Revision 1.1.” The sample size for this measurement is 10^6 UI. This value can be increased to 63 ps for simulation purposes at a BER of 10^{-12}.

NOTES 5: The values in Table 149 are referenced to an ideal 100 Ω differential load at the end of an isolated 3-inch long 85 Ω differential trace behind a standard PCI Express connector. Exact conditions required

for verifying compliance while generating this eye diagram are given in the *PHY Electrical Test Considerations for PCI Express Architecture* document.

Test Procedure

Follow the procedure in “Running Add-In Card Tests" on page 229, and select “Peak Differential Output Voltage”.

Pass Condition

$0.8\ V \le V_{TX-DIFF-p-p} \le 1.2V$

Measurement Algorithm

The Differential Peak Voltage measurement returns two times the larger of the Min or Max statistic if the differential voltage waveform.

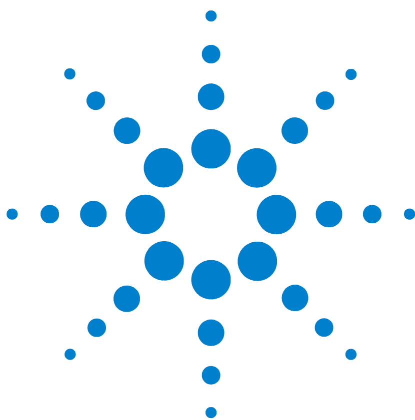
$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}), Min(V_{DIFF(i)}))$$

Where:

i is the index of all waveform values.
V_{DIFF} is the Differential Voltage signal.

Test References

Table 4-7, Section 4.7.1, PCI Express Base Specification v2.0.



15
System Board (Tx) Tests, 2.5 GT/s, PCI-E 2.0

Probing the Link for System Board Compliance 238
Running System Board Tests 240

This section provides the Methods of Implementation (MOIs) for System Board Transmitter tests using an Agilent 54855A, 80000B, or 90000A series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

Probing the Link for System Board Compliance

Connecting the Signal Quality Load Board for System/Motherboard Testing

There are multiple pairs of SMA connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1 With the system/motherboard powered off, connect the Compliance PCI Express Signal Quality Load Board into the connector under test. The PCI Express Signal Quality Load Board has edge fingers for x1, x4, x8 and x16 connectors.

   The PCI Express Signal Quality Load Board will cause a PCI Express 1.1 Base Specification System/motherboard to enter the compliance sub-state of the polling state. During this state the device under test will repeatedly send out the compliance pattern defined in the PCI Express Base Specification.

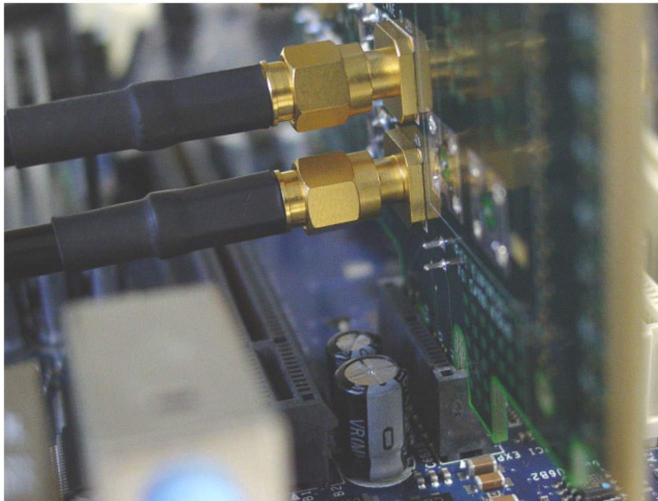


Figure 70 SMA Probing Option

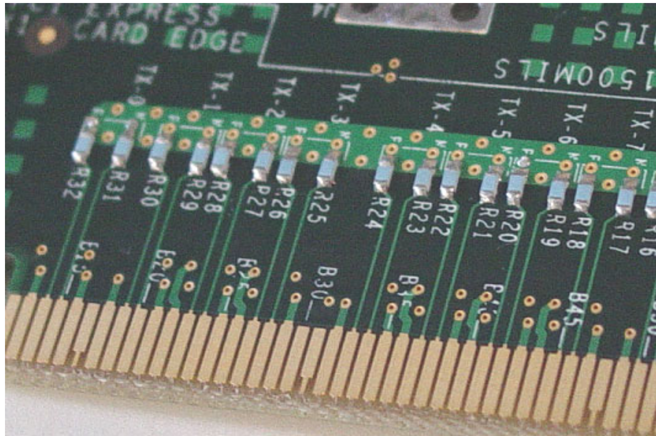


Figure 71 Resistor Terminations for Lanes without SMA Probing

2 Connect cables up as follows:

- **a** Digital Storage Oscilloscope channel 1 to TX LANE 1 P (where Lane 1 is under test).
- **b** Digital Storage Oscilloscope channel 3 to TX LANE 1 N (where Lane 1 is under test).

When SMA probing and two channels are used, channel-to-channel deskew is required (see “Channel-to-Channel De-skew" on page 386).

Not all lanes have SMA probing options. For signal quality testing of the remaining lanes you will need to use a high bandwidth differential or single ended probes (see Figure 46 on page 158). For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 392.

When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the 1134A probe amplifier.

When using a single differential probe head, use oscilloscope channel 2.

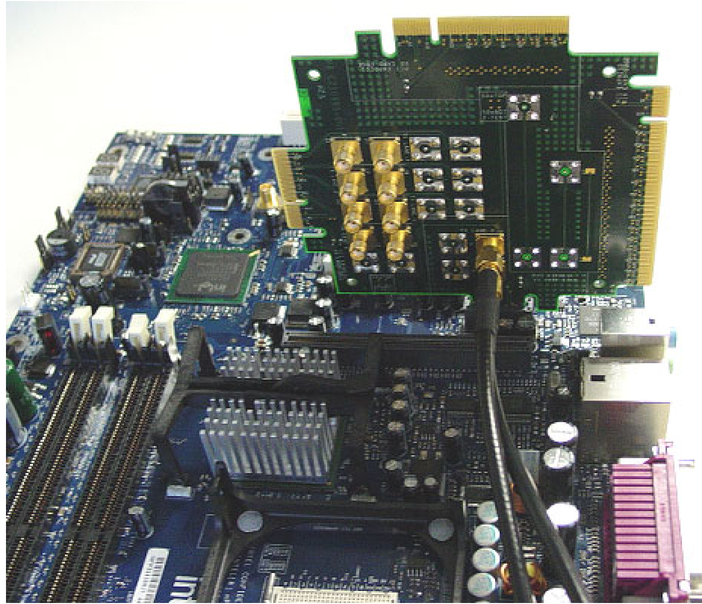


Figure 72 Connecting the PCI Express Signal Quality Test Fixture

Running System Board Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 22. Then, when selecting tests, navigate to the "System Board (Tx) Tests" group.

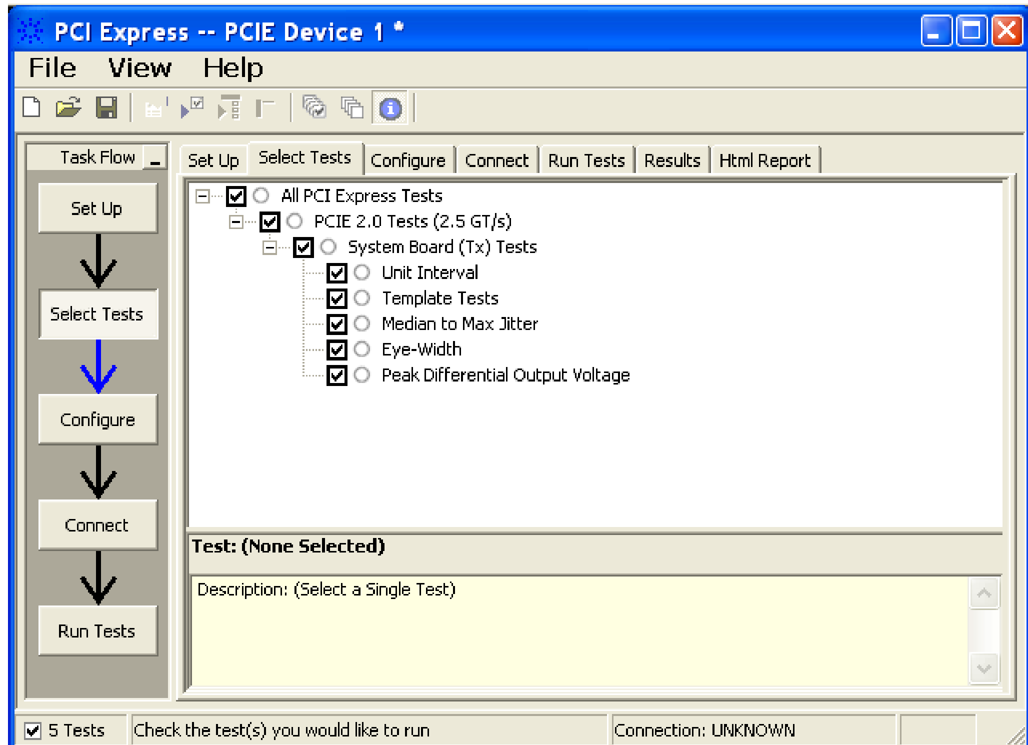


Figure 73 Selecting System Board (Tx) Tests

System Board Tx, Unit Interval

Test Definition Notes from the Specification

Table 150 Unit Interval from Table 4-9 of the Base Specification: 2.5 and 5.0 GT/s Transmitter Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
UI	Unit Interval	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)	ps	The specified UI is equivalent to a tolerance of ±300 ppm for each Refclk source. Period does not account for SSC caused variations. See below note.

- NOTE: SSC permits a +0, -5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33 kHz.

Test Procedure

Follow the procedure in “Running System Board Tests" on page 240, and select “Unit Interval”.

Pass Condition

399.88ps < UI < 400.12ps

Measurement Algorithm

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window.

TX UI(p) = Mean(UI(n))

Where:

n is the index of UI in the clock recovery window.

p indicates the pth 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI, as described below.

NOTE The UI measurement is not required at this point. It is provided as an informative test only.

NOTE The TX UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another TX UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case TX UI is reported.

Test References

Table 4-9, Section 4.3.3.5, PCI Express Base Specification v2.0.

System Board Tx, Template Tests

Test Definition Notes from the Specification

Table 151 System-Board Transmitter Path Compliance Eye Requirements at 2.5 GT/s from Table 4-14 of the Base Specification

Parameter	Min	Max	Unit	Comments
V_{TXS}	274	1200	mV	Notes 1, 2, 5
V_{TXS_d}	253	1200	mV	Notes 1, 2, 5

NOTES 1: An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram.

NOTES 2: Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages.

NOTES 3: T_{TXS} is the minimum eye width. The sample size for this measurement is 10^6 UI. This value can be reduced to 233 ps for simulation purpose at BER 10^{-12}.

NOTE 4: $J_{TXA-MDEDIAN-to-MAX-JITTER}$ is the maximum median-to-peak jitter outlier as defined in the “PCI Express Base Specification, Revision 1.1.” The sample size for this measurement is 10^6 UI. This value can be increased to 83.5 ps for simulation purposes at a BER of 10^{-12}.

NOTES 5: The values in Table 151 are referenced to an ideal 100 Ω differential load at the end of an isolated 3-inch long 85 Ω differential trace behind a standard PCI Express edge finger. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PHY Electrical Test Considerations for PCI Express Architecture* document.

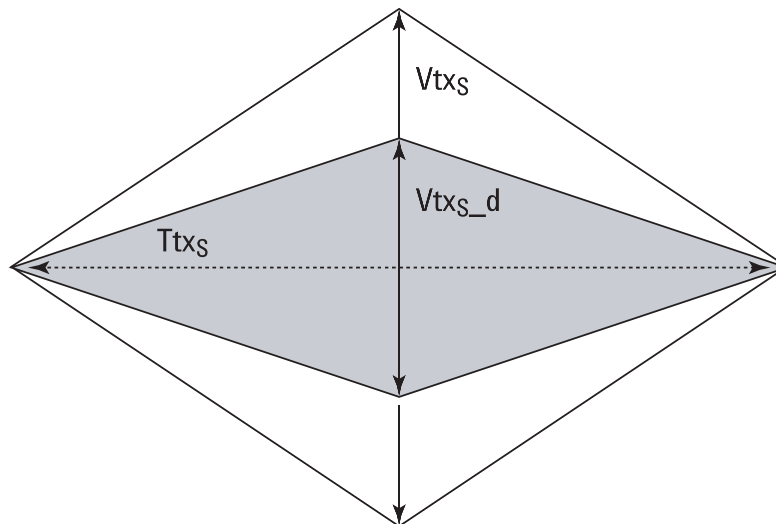


Figure 74 System Board Tx Compliance Eye Diagram

Test References

Table 4-14, Section 4.7.5, PCI Express Base Specification v2.0.

Median to Max Jitter

Test Definition Notes from the Specification

Table 152 System-Board Transmitter Path Compliance Eye Requirements at 2.5 GT/s from Table 4-14 of the Base Specification

Parameter	Min	Max	Unit	Comments
T_{TXS}	246		ps	Notes 1, 3, 5
$J_{TXS\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	108		ps	

NOTES 1: An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram.

NOTES 2: Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages.

NOTES 3: T_{TXS} is the minimum eye width. The sample size for this measurement is 10^6 UI. This value can be reduced to 233 ps for simulation purpose at BER 10^{-12}.

NOTE 4: $J_{TXA\text{-}MDEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ is the maximum median-to-peak jitter outlier as defined in the “PCI Express Base Specification, Revision 1.1.” The sample size for this measurement is 10^6 UI. This value can be increased to 83.5 ps for simulation purposes at a BER of 10^{-12}.

NOTES 5: The values in Table 151 are referenced to an ideal 100 Ω differential load at the end of an isolated 3-inch long 85 Ω differential trace behind a standard PCI Express edge finger. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PHY Electrical Test Considerations for PCI Express Architecture* document.

Limits

Maximum = 77 ps

Pass Condition

77 ps > $T_{TXS\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$.

Test Procedure

Follow the procedure in "Running System Board Tests" on page 240, and select "Median to Max Jitter".

Measurement Algorithm

This measurement is made over 250 consecutive bits defined in Section 3.4 of the Base Specification.

The measured time difference between a data edge and a recovered clock edge.

$tie(n) = t_{R\text{-}DAT}(n) - t_{DAT}(n)$

Where:

t_{DAT} is the original data edge.

$t_{R\text{-}DAT}$ is the recovered data edge (the ideal time of the data edge as defined by the recovered clock around t_{DAT}).

n is the index of all edges in the waveform.

Test References

Table 4-14, Section 4.7.5, PCI Express Base Specification v2.0.

Eye-Width

Test Definition Notes from the Specification

Table 153 System-Board Transmitter Path Compliance Eye Requirements at 2.5 GT/s from Table 4-14 of the Base Specification

Parameter	Min	Max	Unit	Comments
T_{TXS}	246		ps	Notes 1, 3, 5
$J_{TXS\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	108		ps	

NOTES 1: An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram.

NOTES 2: Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages.

NOTES 3: T_{TXS} is the minimum eye width. The sample size for this measurement is 10^6 UI. This value can be reduced to 233 ps for simulation purpose at BER 10^{-12}.

NOTE 4: $J_{TXA-MDEDIAN-to-MAX-JITTER}$ is the maximum median-to-peak jitter outlier as defined in the “PCI Express Base Specification, Revision 1.1.” The sample size for this measurement is 10^6 UI. This value can be increased to 83.5 ps for simulation purposes at a BER of 10^{-12}.

NOTES 5: The values in Table 151 are referenced to an ideal 100 Ω differential load at the end of an isolated 3-inch long 85 Ω differential trace behind a standard PCI Express edge finger. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PHY Electrical Test Considerations for PCI Express Architecture* document.

NOTE

The median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

Limits

Minimum = 246 ps

Pass Condition

246 ps ≤ Ttx_S.

Test Procedure

Follow the procedure in “Running System Board Tests" on page 240, and select “Eye-Width”.

Test References

Table 4-14, Section 4.7.5, PCI Express Base Specification v2.0.

Peak Differential Output Voltage

Test Definition Notes from the Specification

Table 154 System-Board Transmitter Path Compliance Eye Requirements at 2.5 GT/s from Table 4-14 of the Base Specification

Parameter	Min	Max	Unit	Comments
V_{TXS}	274	1200	mV	Notes 1, 2, 5
V_{TXS_d}	253	1200	mV	Notes 1, 2, 5

NOTES 1: An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram.

NOTES 2: Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages.

NOTES 3: T_{TXS} is the minimum eye width. The sample size for this measurement is 10^6 UI. This value can be reduced to 233 ps for simulation purpose at BER 10^{-12}.

NOTE 4: $J_{TXA-MDEDIAN-to-MAX-JITTER}$ is the maximum median-to-peak jitter outlier as defined in the "PCI Express Base Specification, Revision 1.1." The sample size for this measurement is 10^6 UI. This value can be increased to 83.5 ps for simulation purposes at a BER of 10^{-12}.

NOTES 5: The values in Table 154 are referenced to an ideal 100 Ω differential load at the end of an isolated 3-inch long 85 Ω differential trace behind a standard PCI Express edge finger. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PHY Electrical Test Considerations for PCI Express Architecture* document.

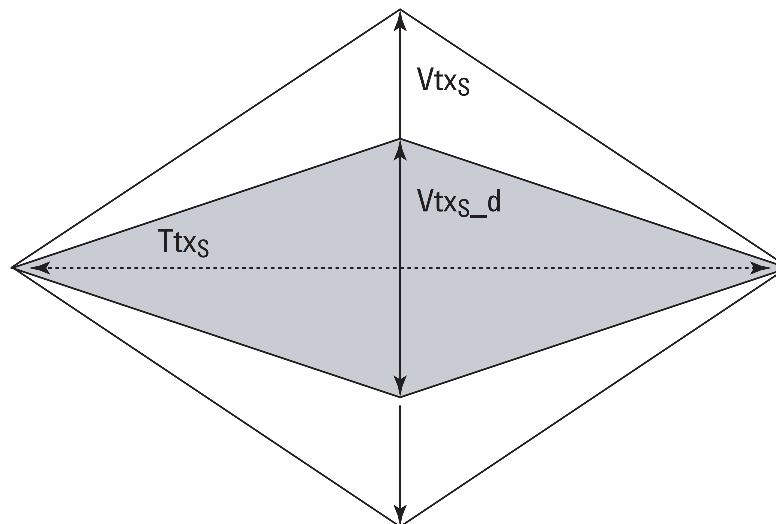


Figure 75 System Board Tx Compliance Eye Diagram

Test Procedure

Follow the procedure in "Running System Board Tests" on page 240, and select "Peak Differential Output Voltage".

Pass Condition

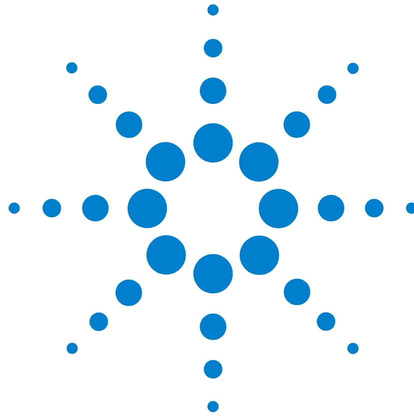
$0.253\ V \le V_{TX\text{-}DIFF\text{-}p\text{-}p} \le 1.200\ V$

Measurement Algorithm.

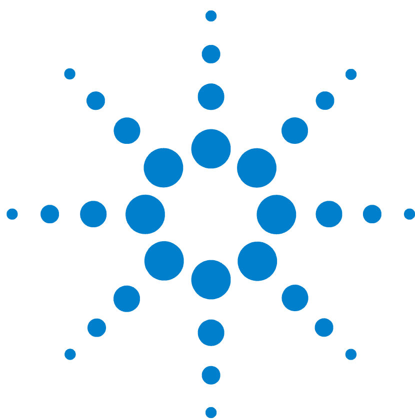
$$V_{TXS\text{-}DIFFp\text{-}p} = 2 \times |V_{TXS\text{-}D+} - V_{TXS\text{-}DIFF\text{-}}|$$

Test References

Table 4-14, Section 4.7.5, PCI Express Base Specification v2.0.



Part V
5.0 GT/s PCI Express Version 2.0



16
Transmitter (Tx) Tests, 5.0 GT/s, PCI-E 2.0

Probing the Link for Tx Compliance 252
Tx Compliance Test Load 256
Running Tx Tests 256

This section provides the Methods of Implementation (MOIs) for Transmitter (Tx) 5.0 GT/s tests of PCI-E 2.0 using an Agilent 80000B or 90000A series Infiniium oscilloscope, 1169A probes, and the PCI Express Automated Test Application.

Probing the Link for Tx Compliance

Transmitter tests are done by connecting the device under test to a test fixture and probing the SMA connectors on the test fixture. To probe the transmitter link, you can:

- Use two 50-ohm coax cables with SMA male connectors, two precision 3.5 mm BNC to SMA male adapters (54855-67604, included with the 54855A oscilloscope), and the Ch1 and Ch3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.
- Use two differential probe heads with two 1169A probe amplifiers (with the negative lead grounded for single-ended measurements) and the Ch1 and Ch3 inputs of an oscilloscope that has 40 GS/s sample rate available on two channels.
- Use one differential probe head with the 1169A probe amplifier and the Ch2 input of an oscilloscope that has 40 GS/s sample rate available on that channel.

When the link is broken and terminated into a 50 ohm load (by the test load), the Compliance Pattern defined in section 4.2.8 (Base Specification) will be transmitted.

Table 155 Probing Options for Transmitter Testing

	Probing Configurations			Captured Waveforms		System Specifications	
						80000B/90000A	
	Probing Method	**Break Serial Link**	**Channels Used**	**Differential Mode**	**Common Mode**	**System Band Width**	**Rise* Time (20-80)**
DUT Connection	Single-Ended SMA (2 x 50-Ohm SMA Cables)	Y	2	Pseudo	Yes	12 GHz	70 ps
	Single-Ended (2 x 1169A w/ Differential Probe Heads)	Y/N	2	Pseudo	Yes	12 GHz	70 ps
	Differential (1 x 1169A w/ Differential Probe Head)	Y/N	1	True	No	12 GHz	70 ps

*Typical

Single-Ended SMA Probing (Ch1) and (Ch3)

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Ch1-Ch3. The Common mode measurements are also available in this configuration from the common mode waveform (Ch1+Ch3)/2.

This probing technique requires breaking the link and terminating into the 50 ohm/side termination into the oscilloscope. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Channel-to-Channel de-skew is required using this technique because two channels are used.

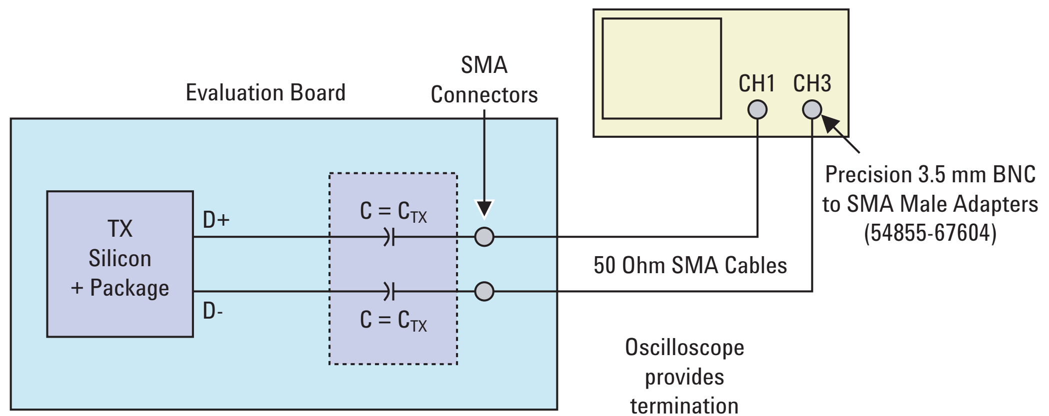


Figure 76 Single-Ended SMA Probing

Single-Ended Probing (Ch1) and (Ch3)

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Ch1-Ch3. The Common mode measurements are also available in this configuration from the common mode waveform (Ch1+Ch3)/2.

Make sure to probe equal distances from the transmitter, as close as possible to the transmitter.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Channel-to-Channel de-skew is required using this technique because two channels are used.

For more information on the 1169A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 392.

Place single-ended grounds as close to the signal line’s reference ground as possible.

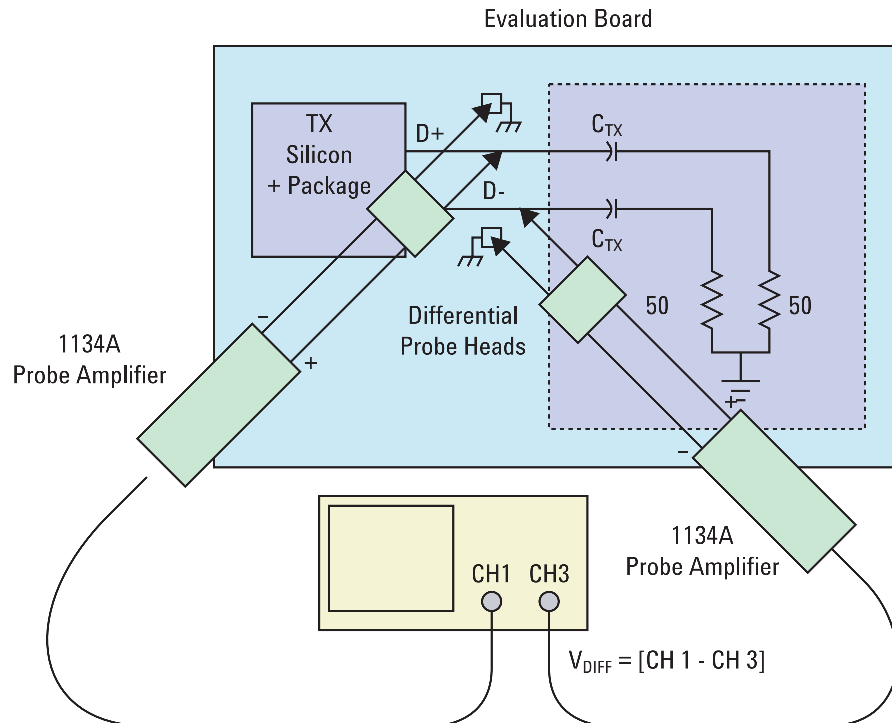


Figure 77 Single-Ended Probing

Differential Probing (Ch2)

The differential signal is measured directly by the differential probe head.

Make sure to probe equal distances from the transmitter, as close as possible to the transmitter.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Only one channel of the oscilloscope is used.

For more information on the 1169A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 392.

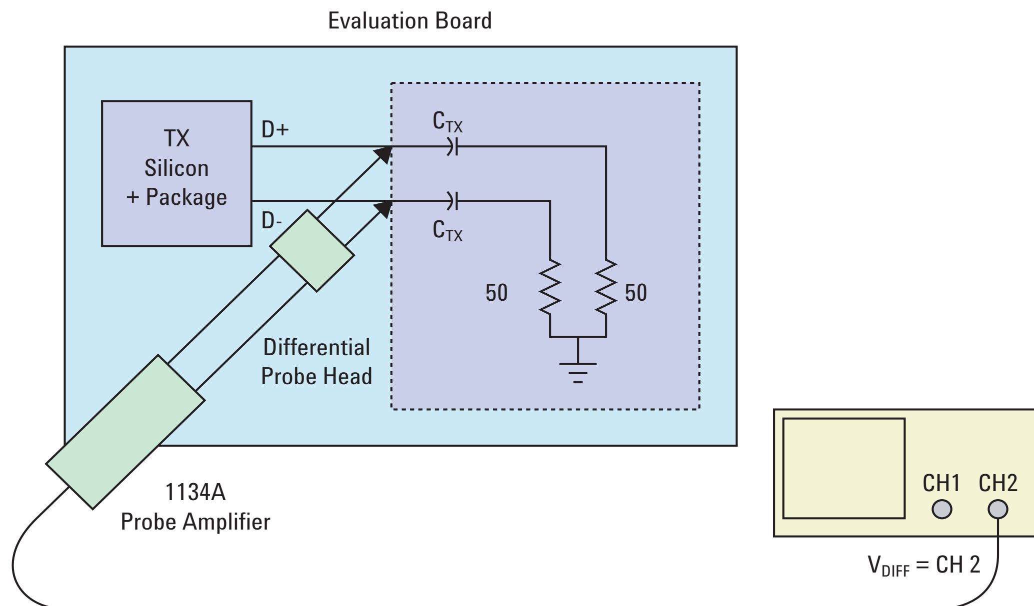


Figure 78 Differential Probing

Tx Compliance Test Load

The compliance test load for driver compliance is shown in Figure 4-25 (Base Specification)

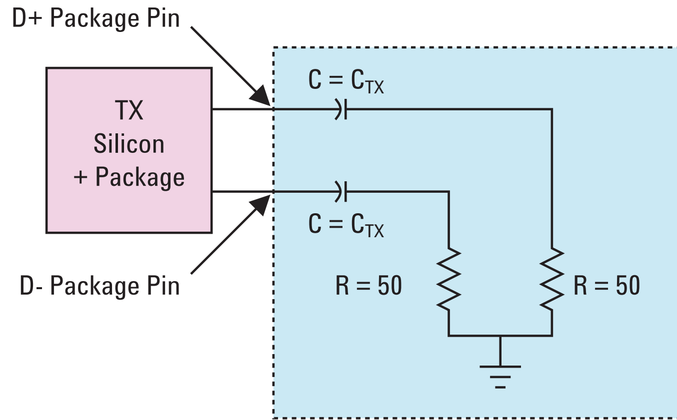


Figure 79 Driver Compliance Test Load.

Running Tx Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 22. Then, when selecting tests, navigate to "Transmitter (Tx) Tests" in the "PCIE 2.0 Tests" group.

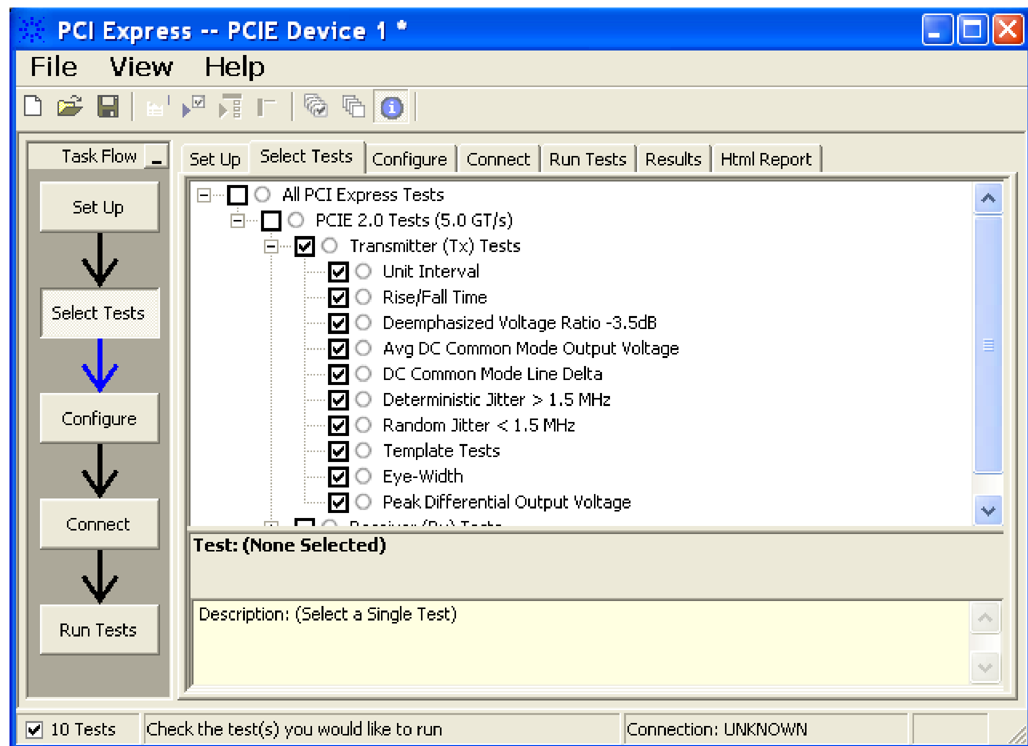


Figure 80 Selecting Transmitter (Tx) Tests

Tx, Unit Interval

Test ID #:

2100

Test Definition Notes from the Specification

Table 156 UI from Table 4-9 of the Base Specification: 2.5 and 5.0 GT/s Transmitter Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
UI	Unit Interval	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)	ps	The specified UI is equivalent to a tolerance of ±300 ppm for each Refclk source. Period does not account for SSC induced variations. See Note 1.

NOTE: SSC permits a +0, -5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33 kHz.

UI is defined in PCI Express Base Specification v2.0, Section 4.3.3.5 and Table 4-9.

Test Procedure

1 Set the probe point to TX_2_0.
2 Perform the PreTest function (Utils.xml).
- construct the extended FW test steps (e.g. CUST_GetMeasStatsStep, CUST_CancelChecker, etc.)

3 Perform the input signal scaling for display optimization and check the signal characteristics.
- this portion is only done if any of the following item changes:
  - probe point (e.g. TX, RX, etc.).
  - the user selectable signal source on the GUI configuration page.
  - the de-embed value on the GUI configuration page.
  - the lane number on the GUI configuration page.
- consist of the probe external scaling to cater for the signal de-embed option.
- vertical auto-scaling of input signal.
- initialize the FUNC2 as differential source.
- verify if the triggers exist.
- verify that the minimum signal pulse width is within 1 UI range (for NON-RefClk test ONLY).
- verify that the maximum signal pulse width is within 5 UI range (for NON-RefClk test ONLY).

4 Setup the labels and grid display settings on the oscilloscope (SetupUI.cmd).
5 Sets the scale and offset of the input channels to their optimum values.
6 Sets the Sample Rate, Enhanced BW, and Memory Depth to the values requested on the configuration page of the GUI.
7 Sets the trigger source and trigger level defined by the user on the configuration page of the GUI.
8 Fit and display all data sample data on the screen.
9 Use the "Unit Interval" measurement on the scope (EZJit option) and the jitter TREND function.
10 Use marker to indicate the upper and lower limit on the FUNC3 (Trend data of UI measurements).
11 Measure the UI_max, UI_min and UI_average from the FUNC3.
12 Report the measurement results.

Measurement Algorithm

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window.

TX UI(p) = Mean(UI(n))

Where:

n is the index of UI in the current 3500 UI clock recovery window.

p indicates the pth 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI, as described below.

NOTE The TX UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another TX UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The mean TX UI is reported.

Test References

- Table 4-9, PCI Express Base Specification v2.0.

Tx, Rise/Fall Time

Test ID #:

2150

Test Definition Notes from the Specification

Table 157 Rise/Fall Time from Table 4-9 of the Base Specification: 2.5 and 5.0 GT/s Transmitter Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$T_{TX-RISE-FALL}$	Transmitter rise and fall time	0.125 (min)	0.15 (min)	UI	Measured differently from 20% to 80% of swing. See below Note and Table 161.

NOTE: Measurements at 5.0 GT/s require an oscilloscope with a bandwidth of ≥ 12.5 GHz, or equivalent, while measurements made at 2.5 GT/s require a scope with at least 6.2 GHz bandwidth. Measurement at 5.0 GT/s must de-convolve effects of compliance test board to yield an effective measurement at Tx pins. 2.5 GT/s may be measured within 200 mils of Tx device's pins, although de-convolution is recommended. For measurement setup details, refer to below figure. At least 10^5 UI of data must be acquired.

Tx, Rise/Fall Time is defined in PCI Express Base Specification v2.0, Section 4.3.3.5 and Table 4-9.

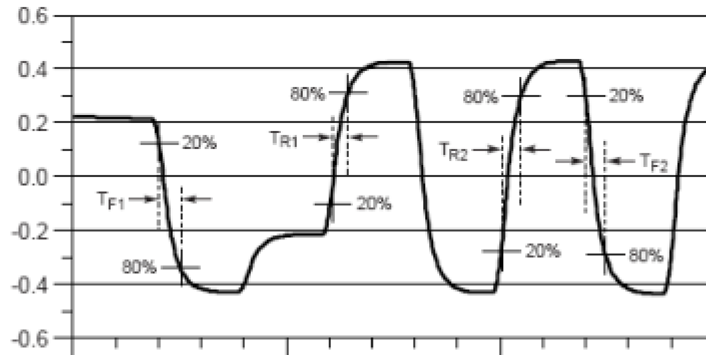


Figure 81 Rise and Fall Time Definitions

Test Procedure

1. Set the probe point to TX_2_0.
2. Perform the PreTest function (Utils.xml).
   - construct the extended FW test steps (e.g. CUST_GetMeasStatsStep, CUST_CancelChecker, etc.)
3. Perform the input signal scaling for display optimization and check the signal characteristics.
   - This portion is only done if any of the following item changes:
     - probe point (e.g. TX, RX, etc.).
     - the user selectable signal source on the GUI configuration page.
     - the de-embed value on the GUI configuration page.
     - the lane number on the GUI configuration page.
   - consist of the probe external scaling to cater for the signal de-embed option.
   - vertical auto-scaling of the input signal.
   - initialize the FUNC2 as differential source.
   - verify if the triggers exist.
   - verify that the minimum signal pulse width is within the 1 UI range (for NON-RefClk test ONLY).
   - verify that the maximum signal pulse width is within the 5 UI range (for NON-RefClk test ONLY).
4. Sets the scale and offset of the input channels to their optimum values.

5 Sets the trigger source and trigger level defined by the user on the configuration page of the GUI.
6 Measure the eye top and base using the histogram.
7 *SetupRiseFallDifferential.cmd* or *SetupRiseFallSingleEnded.cmd:*
   - setup labels and grid display settings on the oscilloscope.
   - enable the RiseTime and FallTime measurements for single ended input channels.
   - enable the de-emphasis measurement for the differential waveform (FUNC2). This measurement value(s) will be used as test results for the De-emphasis Voltage Ratio test.
   - set the timescale to 5 ns.
8 Configure the measurement thresholds settings:
   - 20% - 50% - 80% for the threshold values.
   - define the measurement top/base values (using the previously measured eye top and base using the histogram function).
   - 0V +/- 100mV hysteresis settings for the de-emphasis measurement of the FUNC2.
9 If the "Transition Time Threshold" configuration setting is "Fixed":
   a Enable the jitter mode to turn on the ability to measure all the edges in the waveform and not just the first edge on the screen.
   b Use the test step "GetMeasStatsStep" to obtain all the statistical measurement values that have been enabled previously (RiseTime, FallTime, and De-emphasis).

   If the "Transition Time Threshold" configuration setting is "Variable":
   a Scale the screen to show -1 to 1 UI.
   b Enable the rise time and fall time measurement.
   c Run the oscilloscope until it captures 2,000 edges of rise time/fall time measurement.
10 Find the minimum value from the minimum RiseTime and the minimum FallTime. This value will be used to compare against the specification limits.
11 Report the measurement results:
   - report the total edges used to perform the RiseTime and FallTime measurements.
   - report the minimum FallTime and the minimum RiseTime measured.

Measurement Algorithms

Rise/Fall time is limited to only rising or falling edges of consecutive transitions for transmitter measurements. Rise/Fall Time is taken independently on each single ended waveform sources when you use two single ended probes or two SMA cables as the signal source. Differential signal Rise/Fall Time show up when you select Differential probe type.

Rise Time. The Rise Time measurement is the time difference between when the V_{REF-HI} reference level is crossed and the $V_{REF-LOW}$ reference level is crossed on the rising edge of the waveform.

$t_{RISE}(n) = t_{HI+}(i) - t_{LO+}(j)$

Where:

t_{RISE} is a Rise Time measurement.

t_{HI+} is a set of t_{HI} for rising edges only.

t_{LO+} is a set of t_{LO} for rising edges only.

i and j are indexes for nearest adjacent pairs of t_{LO+} and t_{HI+}.

n is the index of rising edges in the waveform.

Fall Time. The Fall Time measurement is the time difference between when the VREF-HI reference level is crossed and the VREF-LOW reference level is crossed on the falling edge of the waveform.

$t_{FALL}(n) = t_{LO-}(i) - t_{HI-}(j)$

Where:

t_{FALL} is a Fall Time measurement.

t_{HI-} is set of t_{HI} for falling edge only.

t_{LO-} is set of t_{LO} for falling edge only.

i and j are indexes for nearest adjacent pairs of t_{LO-} and t_{HI-}.

n is the index of falling edges in the waveform.

Test References

Table 4-9, PCI Express Base Specification v2.0.

Tx, De-emphasized Voltage Ratio

Test ID #:

2162 (-3.5 dB);

2164 (-6.0 dB)

Test Definition Notes from the Specification

Table 158 De-emphasized Voltage Ratio from Table 4-9 of the Base Specification: 2.5 and 5.0 GT/s Transmitter Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$V_{TX\text{-}DE\text{-}RATIO\text{-}3.5dB}$	Tx de-emphasis level ratio	3.0 (min) 4.0 (max)	3.0 (min) 4.0 (max)	dB	See Section 4.3.3.9 and Note 11 for details.
$V_{TX\text{-}DE\text{-}RATIO\text{-}6dB}$	Tx de-emphasis level ratio	N/A	5.5 (min) 6.5 (max)	dB	See Section 4.3.3.9 and Note 11 for details.

NOTE: Root complex Tx de-emphasis is configured from Upstream controller. Downstream Tx de-emphasis is set via a command, issued at 2.5 GT/s. For details, refer to the appropriate location in Section 4.2.

Tx, De-emphasized Voltage Ratio is defined in PCI Express Base Specification v2.0, Section 4.3.3.5 and Table 4-9.

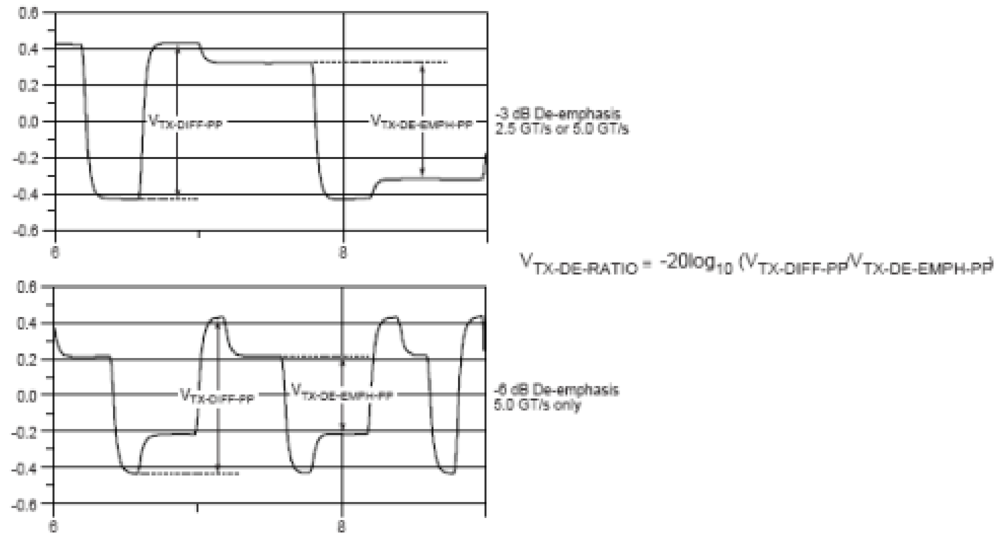


Figure 82 De-emphasized Voltage Ratio Definitions

Test Procedure

1 This test requires the following pre-requisite test(s).

- Rise/Fall Time Test (Test ID: 2150).

2 Set the probe point to TX_2_0.

3 Perform the PreTest function (Utils.xml).

- construct the extended FW test steps (e.g. CUST_GetMeasStatsStep, CUST_CancelChecker, etc.).

4 Perform the input signal scaling for the display optimization and check the signal characteristics.

- This portion is only done if any of the following item changes:
  - probe point (e.g. TX, RX, etc.).
  - The user selectable signal source on the GUI configuration page.
  - The de-embed value on the GUI configuration page.
  - The lane number on the GUI configuration page.
- consist of the probe external scaling to cater for the signal de-embed option.
- vertical auto-scaling of the input signal.
- initialize the FUNC2 as differential source.
- verify if the triggers exist.
- verify that the minimum signal pulse width is within the 1 UI range (for NON-RefClk test ONLY).

- verify that the maximum signal pulse width is within the 5 UI range (for NON-RefClk test ONLY).

5 Report the de-emphasis measurement results obtained from running the pre-requisite test of the Rise/Fall Time Test.

- de-emphasis Min, de-emphasis Max and de-emphasis Mean value.
- minimum de-emphasis value is used as the worst case value.
- de-emphasis mean value is used to compared against the compliance specification limits.

6 Compute the de-emphasis margin values using the framework custom step *margin(...)* function.

Measurement Algorithm

This measurement value is the ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition is divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition.

There are 2 different test IDs for the De-emphasized Voltage Ratio Tests as follow. The test procedure is the same for these tests with the exception of the compliance test limits used for the -3.5dB and the-6.0dB.

a. Tx, De-emphasized Voltage Ratio -3.5dB (PCIE 2.0): ID# 2162

b. Tx, De-emphasized Voltage Ratio -6.0dB (PCIE 2.0): ID# 2164

Test References

Table 4-9, PCI Express Base Specification v2.0.

Tx, Average DC Common Mode Output Voltage

Test ID #:

2180

Test Definition Notes from the Specification

Table 159 Average DC Common Mode Output Voltage from Table 4-9 of the Base Specification: 2.5 and 5.0 GT/s Transmitter Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$V_{TX\text{-}DC\text{-}CM}$	Transmitter DC common-mode voltage	0 (min) 3.6(max)	0 (min) 3.6 (max)	V	The allowed DC common-mode voltage at the Transmitter pins under any conditions.

Tx, Average DC Common Mode Output Voltage is defined in PCI Express Base Specification v2.0, Section 4.3.3.5 and Table 4-9.

Test Procedure

1 Set the probe point to TX_2_0.

2 Perform the PreTest function (Utils.xml).

- construct the extended FW test steps (e.g. CUST_GetMeasStatsStep, CUST_CancelChecker, etc.).

3 Perform input signal scaling for the display optimization and check the signal characteristics.

- this portion is only done if any of the following item changes:
  - probe point (e.g. TX, RX, etc.).
  - the user selectable signal source on the GUI configuration page.
  - the de-embed value on the GUI configuration page.
  - the lane number on the GUI configuration page.
- consist of the probe external scaling to cater for the signal de-embed option.
- vertical auto-scaling of the input signal.
- initialize the FUNC2 as differential source.
- verify if the triggers exist.
- verify that the minimum signal pulse width is within the 1 UI range (for NON-RefClk test ONLY).
- verify that the maximum signal pulse width is within the 5 UI range (for NON-RefClk test ONLY).

4 Sets the scale and offset of the input channels to their optimum values.

5 *SetupDcCommolnModeVoltage.cmd*

- set the timescale to 20ns.
- enable and display the common mode measurements for the FUNC2.
- enable the average common mode measurement.
- use markers to indicate the compliance test limit boundaries (0V to 3.6V).
- setup labels and grid display settings on the oscilloscope.

6 Sets the Sample Rate, Enhanced BW, and Memory Depth to the values requested on the configuration page of the GUI.

7 Sets the trigger source and trigger level defined by the user on the configuration page of the GUI.

8 Use the "WindowDataStep" to display the entire waveform on the screen based on the "ScreenToFullRecordRatio" value.

9 Measure the average common mode result value.
10 Compute the DC Common Mode Line Delta by taking the absolute difference between the average voltage value of the D+ and D- input waveform. This value will be used as the test result for the DC Common Mode Line Delta test.
11 Compare the measured average DC Common Mode value to the compliance test limits.

NOTE

This test is only available when the single-ended or SMA probing method has been used.When the input data is a differential signal (single channel input used), this test will be disabled. (see "Probing the Link for Tx Compliance" on page 252).

Measurement Algorithm

The Average DC Common Mode Voltage measurement computes the DC average of the common mode signal.

$$V_{\text{TX-CM-DC}} = DC_{(avg)} \text{ of } \frac{|V_{\text{TX-D+}} + V_{\text{TX-DC-}}|}{2}$$

The PCIE Base specification states that the transmitter DC common mode voltage must be held at the same value at all states.

Test References

Table 4-9, PCI Express Base Specification v2.0.

Tx, DC Common Mode Line Delta

Test ID #:

2184

Test Definition Notes from the Specification

Table 160 DC Common Mode Line Delta from Table 4-9 of the Base Specification: 2.5 and 5.0 GT/s Transmitter Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0 (min) 25(max)	0 (min) 25 (max)	mV	$\|V_{TX-CM-DC-D+[during\ L0]} - V_{TX-CM-DC-D-[during\ L0]}\| \leq$ 25mV $V_{TX-CM-DC-D}$ - $DC_{(avg)}$ of $_{\|VTX-D+\|}$[during L0] $V_{TX-CM-DC-D}$ - $DC_{(avg)}$ of $_{\|VTX-D-\|}$[during L0]

Tx, DC Common Mode Line Delta is defined in PCI Express Base Specification v2.0, Section 4.3.3.5 and Table 4-9.

Test Procedure

1 This test requires the following pre-requisite test:

- average DC Common Mode Output Voltage Test (Test ID: 2180).

2 Set the probe point to TX_2_0.

3 Perform the PreTest function (Utils.xml).

- construct the extended FW test steps (e.g. CUST_GetMeasStatsStep, CUST_CancelChecker, etc.).

4 Report the measurement results obtained from running the pre-requisite test Average DC Common Mode Output Voltage Test.

- DC Common Mode Line Delta
- average DC value of D+
- average DC value of D-

5 Compare the measured DC Common Mode Line Delta value to the compliance test limits.

NOTE

This test is only available when the single-ended or SMA probing method has been used.When the input data is a differential signal (single channel input used), this test will be disabled. (see "Probing the Link for Tx Compliance" on page 252).

Measurement Algorithm

The DC Common Mode Line Delta measurement computes the absolute difference between the average DC value of the D+ and the average DC value of the D- waveform signals:

$$|V_{TX\text{-}CM\text{-}DC\text{-}D+\ [during\ L0]} - V_{TX\text{-}CM\text{-}DC\text{-}D\text{-}\ [during\ L0.]}| \leq 25\ mV$$

$$V_{TX\text{-}CM\text{-}DC\text{-}D+} = DC_{(avg)}\ of\ |V_{TX\text{-}D+}|\ [during\ L0]$$

$$V_{TX\text{-}CM\text{-}DC\text{-}D-} = DC_{(avg)}\ of\ |V_{TX\text{-}D-}|\ [during\ L0]$$

NOTE The base specification states that $V_{TX\text{-}DC\text{-}CM}$ must be held at the same value during all states. For complete validation, this measurement should be performed on the device in all states and the results compared.

Test References

Table 4-9, PCI Express Base Specification v2.0.

Tx, Deterministic Jitter > 1.5 MHz

Test ID #:

2192

Test Definition Notes from the Specification

Table 161 Deterministic Jitter > 1.5 MHz from Table 4-9 of the Base Specification: 2.5 and 5.0 GT/s Transmitter Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$T_{TX\text{-}HF\text{-}DJ\text{-}DD}$	Tx deterministic jitter > 1.5 MHz	Not specified	0.15 (max)	UI	Deterministic jitter only. See below notes.

NOTE: Measurements at 5.0 GT/s require an oscilloscope with a bandwidth of ≥ 12.5 GHz, or equivalent, while measurements made at 2.5 GT/s require an oscilloscope with at least 6.2 GHz bandwidth. Measurement at 5.0 GT/s must de-convolve effects of compliance test board to yield an effective measurement at Tx pins. 2.5 GT/s may be measured within 200 mils of Tx device's pins, although de-convolution is recommended. At least 10^5 UI of data must be acquired.

NOTE 2: For 5.0 GT/s, de-emphasis timing jitter must be removed. An additional HPF function must be applied. This parameter is measured by accumulating a record length of 10^6 UI while the DUT outputs a compliance pattern. $T_{MIN-PULSE}$ is defined to be nominally 1 UI wide and is bordered on both sides by pulses of the opposite polarity.

Tx, Deterministic Jitter > 1.5 MHz is defined in PCI Express Base Specification v2.0, Section 4.3.3.5 and Table 4-9.

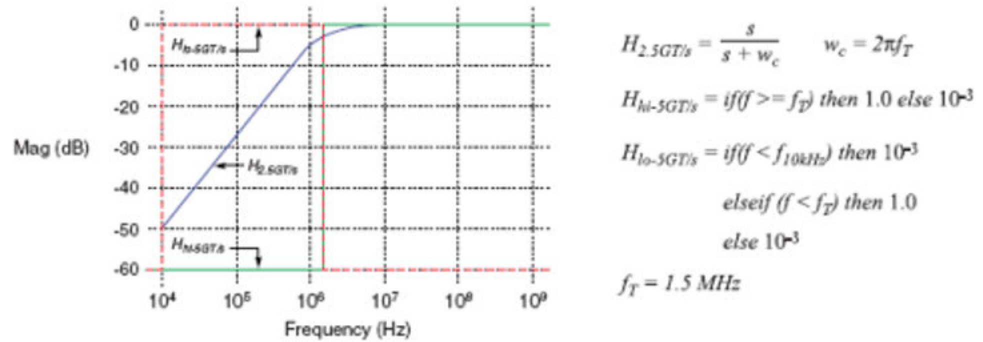


Figure 83 Plot of Transmitter HPF Filter Functions

Test Procedure

1 Set the probe point to TX_2_0.
2 Perform the PreTest function (Utils.xml).

- construct the extended FW test steps (e.g. CUST_GetMeasStatsStep, CUST_CancelChecker, etc.).

3 Perform the input signal scaling for display optimization and check the signal characteristics.

- this portion is only done if any of the following item changes:
    - probe point (e.g. TX, RX, etc.).
    - the user selectable signal source on the GUI configuration page.
    - the de-embed value on the GUI configuration page.
    - the lane number on the GUI configuration page.
- consist of the probe external scaling to cater for the signal de-embed option.
- vertical auto-scaling of input signal.
- initialize the FUNC2 as differential source.
- verify if the triggers exist.
- verify that the minimum signal pulse width is within the 1 UI range (for NON-RefClk test ONLY).

- verify that the maximum signal pulse width is within the 5 UI range (for NON-RefClk test ONLY).

4 Perform the actual compliance testing (CUST_TX_HF_DJ_DD).

- initialize the oscilloscope settings to acquire test waveform data (Scale, Offset, Trigger, Memory depth, etc.).
- initialize the oscilloscope settings for the jitter separation using the EZJIT Plus (TIE brick wall filter settings).
- acquire the oscilloscope sample waveform data (re-iterate to capture at least 1M UI).
- read the test results from the oscilloscope.
- report the test results to ATE Framework.

5 Report the measurement results:

- total number of UIs measured.
- DJ-dd in seconds.
- TJ at BER-12 in seconds.
- RJ_rms in seconds.

6 Compare the measured DJ_dd value to the compliance test limits.

Measurement Algorithm

This is a timing measurement in second generation of PCI Express that requires separation of the high frequency jitter on the transmitter signal.

The transmitter is tested with a low jitter reference clock (clean clock). However, the reference clock may still have some low frequency wander. Besides that, the transmitter itself may have low frequency wander from VDD (supply voltage), temperature and other affects. In order to avoid this increasing observed transmitter jitter, the jitter on the recovered clock is separated into different bands and measured.

1. High frequency jitter (above 1.5 MHz) that is not tracked by the receiver and therefore reduces the transmitter eye width.
2. Low frequency jitter (10kHz - 1.5MHz) that is mostly tracked by the receiver and used as part of the receiver testing.
3. Jitter below 10 kHz that is considered wander or drift and are tracked by the receiver.

This test requires the EZJIT-Plus option to be installed on the scope. The test will be disabled if the option is not available.

Test References

Table 4-9, PCI Express Base Specification v2.0.

Tx, RMS Jitter < 1.5 MHz

Test ID #:

2194

Test Definition Notes from the Specification

Table 162 RMS Jitter < 1.5 MHz from Table 4-9 of the Base Specification: 2.5 and 5.0 GT/s Transmitter Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$T_{TX-LF-RMS}$	Tx RMS jitter < 1.5 MHz	Not specified	3.0	ps RMS	Total energy measured over a 10 kHz - 1.5 MHz range.

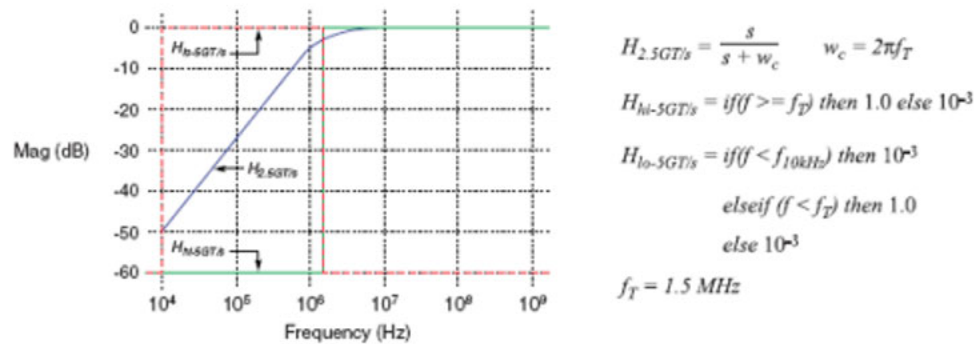


Figure 84 Plot of Transmitter HPF Filter Functions

Test Procedure

1 Set the probe point to TX_2_0.

2 Perform the PreTest function (Utils.xml).

- construct the extended FW test steps (e.g. CUST_GetMeasStatsStep, CUST_CancelChecker, etc.).

3 Perform the input signal scaling for display optimization and check the signal characteristics.

- this portion is only done if any of the following item changes:
  - probe point (e.g. TX, RX, etc.).
  - the user selectable signal source on the GUI configuration page.
  - the de-embed value on the GUI configuration page.
  - the lane number on the GUI configuration page.

- consist of the probe external scaling to cater for the signal de-embed option.
- vertical auto-scaling of input signal.
- initialize the FUNC2 as differential source.
- verify if the triggers exist.
- verify that the minimum signal pulse width is within the 1 UI range (for NON-RefClk test ONLY).
- verify that the maximum signal pulse width is within the 5 UI range (for NON-RefClk test ONLY).

4 Perform the actual compliance testing (CUST_TX_LF_RMS).

- initialize the oscilloscope settings to acquire test waveform data (Scale, Offset, Trigger, Memory depth, etc.).
- initialize the oscilloscope settings for jitter separation using EZJIT Plus (TIE brick wall filter settings).
- acquire the oscilloscope sample waveform data (re-iterate to capture at least 1M UI).
- read the test results from the oscilloscope.
- report the test results to the ATE Framework.

5 Report the measurement results:

- total number of UIs measured.
- DJ-dd in seconds.
- TJ at BER-12 in seconds.
- RJ_rms in seconds.

6 Compare the measured RJ_rms value to the compliance test limits.

Measurement Algorithm

This is a timing measurement in the PCI Express 2 that requires separation of the low frequency jitter on the transmitter signal.

The transmitter is tested with a low jitter reference clock (clean clock). However, the reference clock may still have some low frequency wander. Besides that, the transmitter itself may have low frequency wander from VDD (supply voltage), temperature and other affects. In order to avoid this increasing observed transmitter jitter, jitter on the recovered clock is separated into different bands and measured.

1. High frequency jitter (above 1.5 MHz) that is not tracked by the receiver and therefore reduces the transmitter eye width.
2. Low frequency jitter (10kHz - 1.5MHz) that is mostly tracked by the receiver and used as part of the receiver testing.

3 Jitter below 10 kHz that is considered wander or drift and are tracked by the receiver.

Test References

Table 4-9, PCI Express Base Specification v2.0.

Tx, Template Tests

Test ID #:

2114

Test Definition Notes from the Specification

-

Test Procedure

1 Set the probe point to TX_2_0.

2 Perform the PreTest function (Utils.xml).

- construct the extended FW test steps (e.g. CUST_GetMeasStatsStep, CUST_CancelChecker, etc.).

3 Perform the input signal scaling for display optimization and check the signal characteristics.

- this portion is only done if any of the following item changes:
  - probe point (e.g. TX, RX, etc.).
  - the user selectable signal source on the GUI configuration page.
  - the de-embed value on the GUI configuration page.
  - the lane number on the GUI configuration page.
- consist of the probe external scaling to cater for the signal de-embed option.
- vertical auto-scaling of input signal.
- initialize the FUNC2 as differential source.
- verify if the triggers exist.
- verify that the minimum signal pulse width is within the 1 UI range (for NON-RefClk test ONLY).
- verify that the maximum signal pulse width is within the 5 UI range (for NON-RefClk test ONLY).

4 Perform the actual compliance testing (CUST_SigTestDLL_TxTest).

- check if the "CUST_SigTestDLL_TxTest" has been called in the current trial. This custom test step is designed to execute once per test trial.

- check if the required template file exist. The default template file is "TX_CON.dat", which is modified from the SigTest Add-In Card template file.
- get the framework configuration variables of interest.
- create the plot data directory if it does not exist.
- get the input test waveform data from the oscilloscope (or from Agilent .bin waveform files when running under debug mode only).
- initialize the oscilloscope settings to acquire test waveform data (Scale, Offset, Trigger, Memory depth, etc.).
- acquire the oscilloscope sample waveform data (re-iterate to capture at least 1M UI).
- perform the transmitter compliance test function using the SigTest DLL.
- get the compliance test results from SigTest DLL.
- find and update the worst case test result values.
- calculate the Eye-Width and Differential Peak Output values. These values are used as the final test results in the Eye-Width test and the Differential Peak Output Voltage test.
- report test results to the ATE Framework.
- set flags to indicate that the custom step has been called in the current test trial.

5 Report the measurement results.

6 Display the eye diagrams (transition and non-transition) generated using the SigTest DLL plot data.

7 Check for the mask failures in both transition and non-transition eye diagrams. Test will fail if total failures are not equal to zero.

Measurement Algorithm

All PCI Express Device Types must meet the Transmitter eye diagram as specified in the PCI Express Base Specification.

All Links are assumed active while generating this eye diagram. Transition and non-transition bits must be distinguished in order to measure the compliance against the de-emphasized voltage level.

Test References

Table 4-9, PCI Express Base Specification v2.0.

Tx, Eye Width

Test ID #:

2134

Test Definition Notes from the Specification

Table 163 Eye Width from Table 4-9 of the Base Specification: 2.5 and 5.0 GT/s Transmitter Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
T_{TX-EYE}	Transmitter Eye including all jitter sources	0.75 (min)	0.75 (min)	UI	Does not include SSC or Refclk jitter. Includes Rj at 10^{-12}. See below notes. Note that 2.5 GT/s and 5.0 GT/s use different jitter determination methods.

NOTE: Measurements at 5.0 GT/s require an oscilloscope with a bandwidth of ≥ 12.5 GHz, or equivalent, while measurements made at 2.5 GT/s require an oscilloscope with at least 6.2 GHz bandwidth. Measurement at 5.0 GT/s must de-convolve effects of compliance test board to yield an effective measurement at Tx pins. 2.5 GT/s may be measured within 200 mils of Tx device's pins, although de-convolution is recommended. At least 10^5 UI of data must be acquired.

NOTE 2: Transmitter jitter is measured by driving the Transmitter under tests with a low jitter "ideal" clock and connecting the DUT to a reference load.

NOTE 3: Transmitter raw jitter data must be convolved with a filtering function that represents the worst case CDR tracking BW. 2.5 GT/s and 5.0 GT/s use different filter functions. After the convolution process has been applied, the center of the resulting eye must be determined and used as a reference point for obtaining eye voltage and margins.

NOTE 4: For 5.0 GT/s, de-emphasis timing jitter must be removed. An Additional HPF function must be applied. This parameter is measured by accumulating a record length of 10^6 UI while the DUT outputs a compliance pattern. $T_{MIN-PULSE}$ is defined to be nominally 1 UI wide and is bordered on both sides by pulses of opposite polarity.

Test Procedure

1 Set the probe point to TX_2_0.
2 Perform the PreTest function (Utils.xml).

- construct the extended FW test steps (e.g. CUST_GetMeasStatsStep, CUST_CancelChecker, etc.).

3 Perform the input signal scaling for display optimization and check the signal characteristics.

- this portion is only done if any of the following item changes:
  - probe point (e.g. TX, RX, etc.).
  - the user selectable signal source on the GUI configuration page.
  - the de-embed value on the GUI configuration page.
  - the lane number on the GUI configuration page.
- consist of the probe external scaling to cater for the signal de-embed option.
- vertical auto-scaling of input signal.
- initialize the FUNC2 as differential source.
- verify if the triggers exist.
- verify that the minimum signal pulse width is within the 1 UI range (for NON-RefClk test ONLY).
- verify that the maximum signal pulse width is within the 5 UI range (for NON-RefClk test ONLY).

4 Perform the actual compliance testing (CUST_SigTestDLL_TxTest).

- check if the "CUST_SigTestDLL_TxTest" has been called in the current trial. This custom test step is designed to execute once per test trial.
- check if the required template file exist. The default template file is "TX_CON.dat", which is modified from the SigTest Add-In Card template file.
- get the framework configuration variables of interest.
- create the plot data directory if it does not exist.
- get the input test waveform data from the oscilloscope (or from Agilent .bin waveform files when running under debug mode only).
- initialize the oscilloscope settings to acquire test waveform data (Scale, Offset, Trigger, Memory depth, etc.).
- acquire the oscilloscope sample waveform data (re-iterate to capture at least 1M UI).
- perform the transmitter compliance test function using the SigTest DLL.
- get the compliance test results from SigTest DLL.
- find and update the worst case test result values.

- calculate the Eye-Width and Differential Peak Output values. These values are used as the final test results in the Eye-Width test and the Differential Peak Output Voltage test.
- report test results to the ATE Framework.
- set flags to indicate that the custom step has been called in the current test trial.

5 Report the measurement results.

6 Compare the measured Eye-Width value to the compliance test limits.

Measurement Algorithm

This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [total jitter at BER-12]. This parameter is measured with the equivalent of a zero jitter reference clock.

Test References

Table 4-9, PCI Express Base Specification v2.0.

Tx, Peak Differential Output Voltage

Test ID #:

2144

Test Definition Notes from the Specification

Table 164 Peak Differential Output Voltage from Table 4-9 of the Base Specification: 2.5 and 5.0 GT/s Transmitter Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$T_{TX\text{-}DIFF\text{-}PP}$	Differential p-p Tx voltage swing	0.8 (min) 1.2 (max)	0.8 (min) 1.2 (max)	V	As measured with compliance test load. Defined as $2^*\|V_{TXD+} - V_{TXD-}\|$.

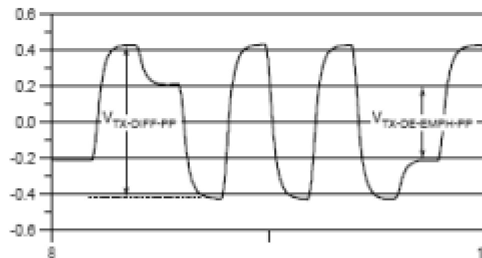


Figure 85 Full Swing Signaling Voltage Parameters Showing -6 dB De-emphasis

Test Procedure

1 Set the probe point to TX_2_0.
2 Perform the PreTest function (Utils.xml).

- construct the extended FW test steps (e.g. CUST_GetMeasStatsStep, CUST_CancelChecker, etc.).

3 Perform the input signal scaling for display optimization and check the signal characteristics.

- this portion is only done if any of the following item changes:
  - probe point (e.g. TX, RX, etc.).
  - the user selectable signal source on the GUI configuration page.
  - the de-embed value on the GUI configuration page.
  - the lane number on the GUI configuration page.
- consist of the probe external scaling to cater for the signal de-embed option.
- vertical auto-scaling of input signal.
- initialize the FUNC2 as differential source.
- verify if the triggers exist.
- verify that the minimum signal pulse width is within the 1 UI range (for NON-RefClk test ONLY).
- verify that the maximum signal pulse width is within the 5 UI range (for NON-RefClk test ONLY).

4 Perform the actual compliance testing (CUST_SigTestDLL_TxTest).

- check if the "CUST_SigTestDLL_TxTest" has been called in the current trial. This custom test step is designed to execute once per test trial.
- check if the required template file exist. The default template file is "TX_CON.dat", which is modified from the SigTest Add-In Card template file.
- get the framework configuration variables of interest.
- create the plot data directory if it does not exist.
- get the input test waveform data from the oscilloscope (or from Agilent .bin waveform files when running under debug mode only).
- initialize the oscilloscope settings to acquire test waveform data (Scale, Offset, Trigger, Memory depth, etc.).
- acquire the oscilloscope sample waveform data (re-iterate to capture at least 1M UI).
- perform the transmitter compliance test function using the SigTest DLL.
- get the compliance test results from SigTest DLL.
- find and update the worst case test result values.

- calculate the Eye-Width and Differential Peak Output values. These values are used as the final test results in the Eye-Width test and the Differential Peak Output Voltage test.
- report test results to the ATE Framework.
- set flags to indicate that the custom step has been called in the current test trial.

5 Report the measurement results.

6 Compare the measured Differential Peak Output Voltage (WorstValue) value to the compliance test limits.

Measurement Algorithm

The Differential Peak Voltage measurement returns twice of the larger voltage among the Min or Max statistic of the differential voltage waveform.

$V_{TX-DIFF-p-p} = 2 * Max\ (\ Max(V_{DIFF(i)}),\ Min(V_{DIFF(i)})\ )$

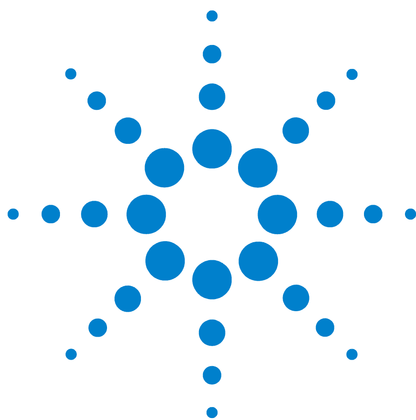
Where:

d i is the index of all waveform values.

e V_{DIFF} is the Differential Voltage signal.

Test References

Table 4-9, PCI Express Base Specification v2.0.



17
Receiver (Rx) Tests, 5.0 GT/s, PCI-E 2.0

Probing the Link for Rx Compliance 282
Running Receiver Tests 285

This section provides the Methods of Implementation (MOIs) for Receiver (Rx) 5.0 GT/s tests of PCI-E 2.0 using an Agilent 80000B or 90000A series Infiniium oscilloscope, 1169A probes, and the PCI Express Automated Test Application.

NOTE None of the included receiver tests validate the receiver's ability to correctly receive data (also known as receiver tolerance). Rather, they validate that the signal as seen by the receiver meets or exceeds various parameters (maximum voltage, jitter, eye width, etc.). These tests validate the transmitter and interconnect. Separate receiver tolerance testing is required to ensure the receiver is correctly receiving data.

Probing the Link for Rx Compliance

Receiver tests are done by probing the link as close as is feasibly possible to the pins of the receiver device. Alternatively, a dummy load can be used for the termination of the link. To probe the receiver link, you can:

- Use two differential probe heads with two 1169A probe amplifiers (with the negative lead grounded for single-ended measurements) and the Ch1 and Ch3 inputs of an oscilloscope that has 40 GS/s sample rate available on two channels.
- Use one differential probe head with the 1169A probe amplifier and the Ch2 input of an oscilloscope that has 40 GS/s sample rate available on that channel.

Table 165 Probing Options for Receiver Testing

<table>
<tr><th rowspan="3"></th><th colspan="3">Probing Configurations</th><th colspan="2">Captured Waveforms</th><th colspan="2">System Specifications</th></tr>
<tr><th rowspan="2">Probing Method</th><th rowspan="2">Break Serial Link</th><th rowspan="2">Channels Used</th><th rowspan="2">Differential Mode</th><th rowspan="2">Common Mode</th><th colspan="2">80000B/90000A</th></tr>
<tr><th>System Band Width</th><th>Rise* Time (20-80)</th></tr>
<tr><td rowspan="2">DUT Connection</td><td>Single-Ended (2 x 1169A w/ Differential Probe Heads)</td><td>Y/N</td><td>2</td><td>Pseudo</td><td>Yes</td><td>12 GHz</td><td>70 ps</td></tr>
<tr><td>Differential (1 x 1169A w/ Differential Probe Head)</td><td>Y/N</td><td>1</td><td>True</td><td>No</td><td>12 GHz</td><td>70 ps</td></tr>
</table>

*Typical

Single-Ended Probing (Ch1) and (Ch3)

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Ch1-Ch3. The Common mode measurements are also available in this configuration from the common mode waveform (Ch1+Ch3)/2.

Make sure to probe equal distances from the receiver, as close as possible to the receiver, with the shortest ground connection possible.

This probing technique can be used for either a live link that is transmitting data, or a link terminated into a "dummy load."

Channel-to-channel de-skew is required using this technique because two channels are used.

For more information on the 1169A probe amplifier and differential probe heads, see Appendix B, "InfiniiMax Probing Options," starting on page 392.

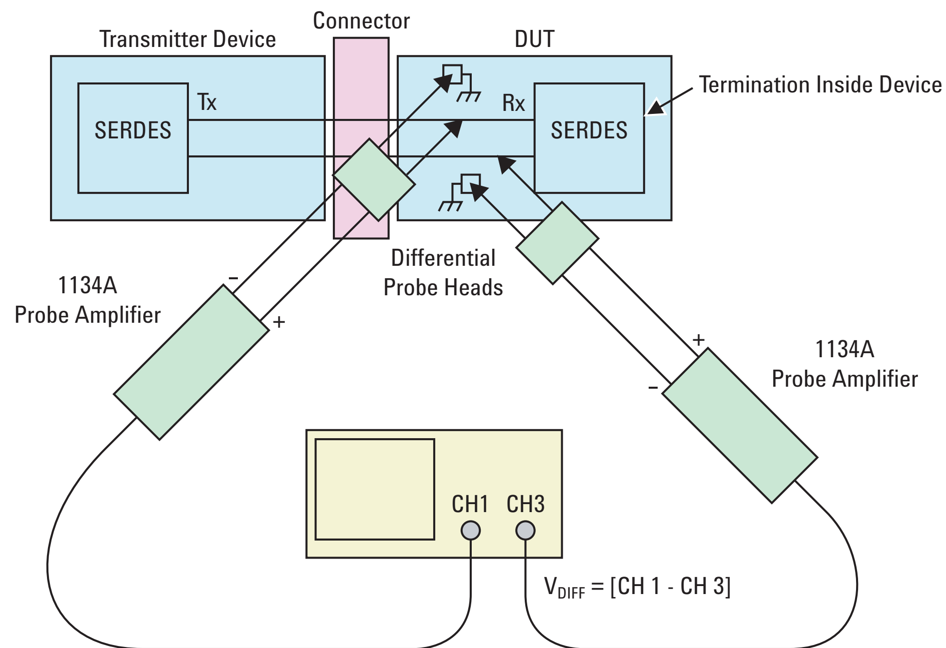


Figure 86 Single-Ended Probing

Differential Probing (Ch2)

The differential signal is measured directly by the differential probe head.

Make sure to probe equal distances from the receiver, as close as possible to the receiver, with the shortest ground connection possible.

This probing technique can be used for either a live link that is transmitting data, or a link terminated into a “dummy load.”

A single channel of the oscilloscope is used, so de-skew is not necessary.

For more information on the 1169A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 392.

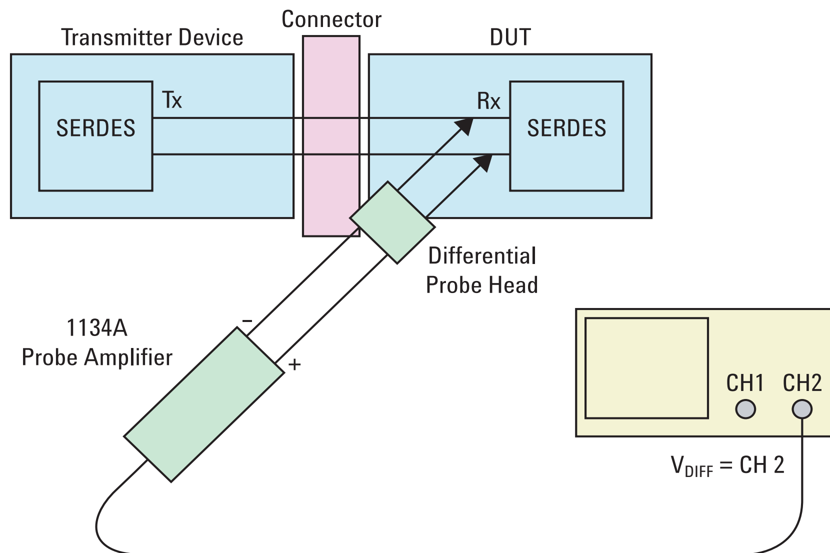


Figure 87 Differential Probing

Running Receiver Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 22. Then, when selecting tests, navigate to the "Receiver (Rx) Tests" group.

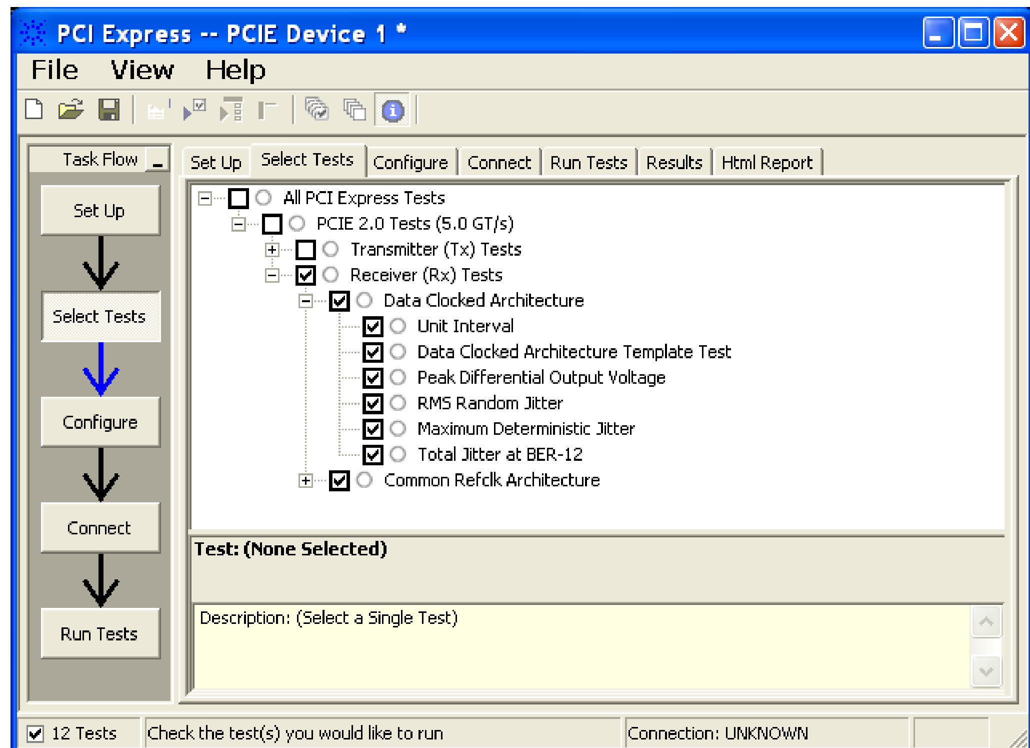


Figure 88 Selecting Receiver (Rx) Tests

Rx, Unit Interval (Data Clocked, Common Refclk)

Test ID #:

2200 - Data Clocked Architecture

2202 - Common Refclk Architecture

Test Definition Notes from the Specification

Table 166 Unit Interval from Table 4-12 of the Base Specification: 2.5 and 5.0 GT/s Receiver Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
UI	Unit Interval	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)	ps	UI does not account for SSC caused variations.

Test Procedure

1 Set the probe point to RX_2_0 for Data Clocked; or RX_CC_2_0 for Common Refclk.

2 Perform PreTest function (Utils.xml)

- construct extended FW test steps (e.g. CUST_GetMeasStatsStep, CUST_CancelChecker, etc.).

3 Perform the input signal scaling for display optimization and check the signal characteristics.

- This portion is only done if any of the following item changes:
  - probe point (e.g. TX, RX, etc.).
  - the user selectable signal source on the GUI configuration page.
  - the de-embed value on the GUI configuration page.
  - the lane number on the GUI configuration page.
- consist of probe external scaling to cater for the signal de-embed option.
- vertical auto-scaling of the input signal.
- initialize the FUNC2 as differential source.
- verify if the triggers exist
- verify that the minimum signal pulse width is within 1 UI range (for NON-RefClk test ONLY).
- verify that the maximum signal pulse width is within 5 UI range (for NON-RefClk test ONLY).

4 Setup the labels and grid display settings on the oscilloscope (SetupUI.cmd).

5 Sets the scale and offset of the input channels to their optimum values.

6 Sets the Sample Rate, Enhanced BW, and Memory Depth to the values requested on the configuration page of the GUI.

7 Sets the trigger source and trigger level defined by the user on the configuration page of the GUI.

8 Fit and display all data sample data on the screen.

9 Use the "Unit Interval" measurement on the oscilloscope (EZJit option) and jitter TREND function.

10 Use the marker to indicate the upper and lower limit on the FUNC3(Trend data of UI measurements).

11 Measure UI_max, UI_min and UI_average from FUNC3.

12 Report measurement results.

Measurement Algorithm

A recovered TX UI is calculated over 3500 consecutive unit intervals of a sample data as the mean unit interval over the clock recovery window.

TX UI(p) = Mean(UI(n))

Where:

n is the index of UI in the clock recovery window.

p indicates the pth 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

NOTE The TX UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another TX UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The mean TX UI is reported.

There are two different test IDs for the Receiver Unit Interval Tests. The test procedure is the same for these tests.

a Rx, Data Clocked Unit Interval (PCIE 2.0): ID# 2200

b Rx, Common Refclk Unit Interval (PCIE 2.0): ID# 2202

Test References

Table 4-12, PCI Express Base Specification v2.0.

Rx, Template Test

Test ID #:

2210 - Data Clocked Architecture

2211 - Common Refclk Architecture

Test Definition Notes from the Specification

-

Test Procedure

1. Set the probe point to RX_2_0 for Data Clocked; or RX_CC_2_0 for Common Refclk.
2. Perform PreTest function (Utils.xml)

- construct extended FW test steps (e.g. CUST_GetMeasStatsStep, CUST_CancelChecker, etc.).

3 Perform the input signal scaling for display optimization and check the signal characteristics.

- This portion is only done if any of the following item changes:
  - probe point (e.g. TX, RX, etc.).
  - the user selectable signal source on the GUI configuration page.
  - the de-embed value on the GUI configuration page.
  - the lane number on the GUI configuration page.
- consist of probe external scaling to cater for the signal de-embed option.
- vertical auto-scaling of the input signal.
- initialize the FUNC2 as differential source.
- verify if the triggers exist
- verify that the minimum signal pulse width is within 1 UI range (for NON-RefClk test ONLY).
- verify that the maximum signal pulse width is within 5 UI range (for NON-RefClk test ONLY).

4 Perform actual compliance testing using the SigTest DLL (CUST_SigTestDLL_RxDataClkTest or CUST_SigTestDLL_RxCommonClkTest)

- check if the custom test step has been called in the current trial. This custom test step is designed to execute once per test trial.
- check if the required template file exist. The default template file is as follow.
  - Data Clocked architecture: "RX_DC_CON.dat" (modified from the SigTest Add-In Card template file).
  - Common Refclk architecture: "RX_CC_CON.dat" (modified from the SigTest System Board template file).
- get the framework configuration variables of interest.
- create plot data directory if it does not exist.
- get the input test waveform data from the oscilloscope (or from Agilent. bin waveform files when running under debug mode only).
- initialize the oscilloscope settings to acquire test waveform data (Scale, Offset, Trigger, Memory depth, etc.).
- acquire the oscilloscope sample waveform data (re-iterate to capture at least 1M UI).
- perform the receiver compliance test function using the SigTest DLL.
- get the compliance test results from SigTest DLL.
- find and update the worst case test result values.

- calculate the Eye-Width and Differential Peak Output values. These values are used as the final test results in the Eye-Width test and the Differential Peak Output Voltage test.
- report the test results to ATE Framework.
- set the flags to indicate that the custom step has been called in the current test trial.

5 Report the measurement results.

6 Display the eye diagrams (transition and non-transition) generated using the SigTest DLL plot data.

7 Check for mask failures in both transition and non-transition eye diagrams. Test will fail if total failures are not equal to zero.

Measurement Algorithm

The Receiver must reliably receive all data that meets the differential receiver input specifications as shown in PCI Express Base Specification, rev 2.0. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specification in the Table 4-12.

All Links are assumed active while generating this eye diagram. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level.

There are 2 different test IDs for the Receiver Template Tests as follow. The test procedure is the same for these tests with the exception of the template files used for the Data Clocked architecture and for the Common Refclk architecture.

a Rx, Data Clocked Architecture Template Test (PCIE 2.0): ID# 2210

b Rx, Common Refclk Architecture Template Test (PCIE 2.0): ID# 2211

Test References

Table 4-12, PCI Express Base Specification v2.0.

The total number of mask violation shall be 0.

Rx, Peak Differential Output Voltage

Test ID #:

2241 - Data Clocked Architecture

2243 - Common Refclk Architecture

Test Definition Notes from the Specification

Table 167 Peak Differential Output Voltage from Table 4-12 of the Base Specification: 2.5 and 5.0 GT/s Receiver Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$V_{RX\text{-}DIFF\text{-}PP\text{-}CC}$	Differential Rx peak-peak voltage for common Refclk Rx architecture	0.175 (min) 1.2 (max)	0.120 (min) 1.2 (max)	V	See Section 4.3.7.2.2.
$V_{RX\text{-}DIFF\text{-}PP\text{-}DC}$	Differential Rx peak-peak voltage for data clocked Rx architecture	0.175 (min) 1.2 (max)	0.100 (min) 1.2 (max)	V	See Section 4.3.7.2.2.

Test Procedure

1 Set the probe point to RX_2_0 for Data Clocked; or RX_CC_2_0 for Common Refclk.

2 Perform PreTest function (Utils.xml)

- construct extended FW test steps (e.g. CUST_GetMeasStatsStep, CUST_CancelChecker, etc.).

3 Perform the input signal scaling for display optimization and check the signal characteristics.

- This portion is only done if any of the following item changes:
  - probe point (e.g. TX, RX, etc.).
  - the user selectable signal source on the GUI configuration page.
  - the de-embed value on the GUI configuration page.
  - the lane number on the GUI configuration page.
- consist of probe external scaling to cater for the signal de-embed option.
- vertical auto-scaling of the input signal.
- initialize the FUNC2 as differential source.
- verify if the triggers exist
- verify that the minimum signal pulse width is within 1 UI range (for NON-RefClk test ONLY).
- verify that the maximum signal pulse width is within 5 UI range (for NON-RefClk test ONLY).

4 Perform actual compliance testing using the SigTest DLL (CUST_SigTestDLL_RxDataClkTest or CUST_SigTestDLL_RxCommonClkTest)

- check if the custom test step has been called in the current trial. This custom test step is designed to execute once per test trial.
- check if the required template file exist. The default template file is as follow.
    - Data Clocked architecture: "RX_DC_CON.dat" (modified from the SigTest Add-In Card template file).
    - Common Refclk architecture: "RX_CC_CON.dat" (modified from the SigTest System Board template file).
- get the framework configuration variables of interest.
- create plot data directory if it does not exist.
- get the input test waveform data from the oscilloscope (or from Agilent .bin waveform files when running under debug mode only).
- initialize the oscilloscope settings to acquire test waveform data (Scale, Offset, Trigger, Memory depth, etc.).
- acquire the oscilloscope sample waveform data (re-iterate to capture at least 1M UI).
- perform the receiver compliance test function using the SigTest DLL.
- get the compliance test results from SigTest DLL.
- find and update the worst case test result values.
- calculate the Eye-Width and Differential Peak Output values. These values are used as the final test results in the Eye-Width test and the Differential Peak Output Voltage test.
- report the test results to ATE Framework.
- set the flags to indicate that the custom step has been called in the current test trial.

5. Report the measurement results.
6. Compare the measured Differential Peak Output Voltage (WorstValue) value to the compliance test limits.

Measurement Algorithm

The Differential Peak Voltage measurement returns twice of the larger voltage among the Min or Max statistic of the differential voltage waveform.

$V_{TX\text{-}DIFF\text{-}p\text{-}p} = 2 * Max(Max(V_{DIFF(i)}), Min(V_{DIFF(i)}))$

Where:

i is the index of all waveform values.

V_{DIFF} is the Differential Voltage signal.

There are 2 different test IDs for Receiver Peak Differential Output Voltage Tests as follow. The test procedure is the same for these tests with the exception of the template files used for the Data Clocked architecture and for the Common Refclk architecture.

a Rx, Data Clocked Architecture Peak Differential Output Voltage (PCIE 2.0): ID# 2241

b Rx, Common Refclk Architecture Peak Differential Output Voltage (PCIE 2.0): ID# 2243

Test References

Table 4-12, PCI Express Base Specification v2.0.

The measured Differential Peak Output Voltage value is within the conformance range limits.

(120mV <= $V_{TX-DIFF-p-p}$ <= 1.2V) for Common Refclk architecture.

(100mV <= $V_{TX-DIFF-p-p}$ <= 1.2V) for Data Clocked architecture.

Rx, RMS Random Jitter

Test ID #:

2282 - Data Clocked Architecture

2284 - Common Refclk Architecture

Test Definition Notes from the Base Specification

The RMS RJ range for this test is NOT specified in the Base specifications. This test is to provide informative data only.

Table 168 RMS Random Jitter from Table 4-12 of the Base Specification: 2.5 and 5.0 GT/s Receiver Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$V_{RX-TJ-CC}$	Max Rx inherent timing error	N/A	0.40 (max)	UI	Max Rx inherent total timing error for common Refclk Rx architecture. See below note.
$V_{RX-TJ-DC}$	Max Rx inherent timing error	N/A	0.34 (max)	UI	Max Rx inherent total timing error for data clocked Rx architecture. See below note.
$V_{RX-DJ-DD-CC}$	Max Rx inherent deterministic timing error	N/A	0.30 (max)	UI	Max Rx inherent deterministic timing error for common Refclk Rx architecture. See below note.

Table 168 RMS Random Jitter from Table 4-12 of the Base Specification: 2.5 and 5.0 GT/s Receiver Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$V_{RX-TJ-DC}$	Max Rx inherent deterministic timing error	N/A	0.24 (max)	UI	Max Rx inherent deterministic timing error for data clocked Rx architecture. See below note.

NOTE: The four inherent timing error parameters are defined for the convenience of Rx designers, and they are measured during Receiver tolerancing.

Test Procedure

1 Set the probe point to RX_2_0 for Data Clocked; or RX_CC_2_0 for Common Refclk.

2 Perform PreTest function (Utils.xml)

- construct extended FW test steps (e.g. CUST_GetMeasStatsStep, CUST_CancelChecker, etc.).

3 Perform the input signal scaling for display optimization and check the signal characteristics.

- This portion is only done if any of the following item changes:
  - probe point (e.g. TX, RX, etc.).
  - the user selectable signal source on the GUI configuration page.
  - the de-embed value on the GUI configuration page.
  - the lane number on the GUI configuration page.
- consist of probe external scaling to cater for the signal de-embed option.
- vertical auto-scaling of the input signal.
- initialize the FUNC2 as differential source.
- verify if the triggers exist
- verify that the minimum signal pulse width is within 1 UI range (for NON-RefClk test ONLY).
- verify that the maximum signal pulse width is within 5 UI range (for NON-RefClk test ONLY).

4 Perform actual compliance testing using the SigTest DLL (CUST_SigTestDLL_RxDataClkTest or CUST_SigTestDLL_RxCommonClkTest)

- check if the custom test step has been called in the current trial. This custom test step is designed to execute once per test trial.

- check if the required template file exist. The default template file is as follow.
  - Data Clocked architecture: "RX_DC_CON.dat" (modified from the SigTest Add-In Card template file).
  - Common Refclk architecture: "RX_CC_CON.dat" (modified from the SigTest System Board template file).
- get the framework configuration variables of interest.
- create plot data directory if it does not exist.
- get the input test waveform data from the oscilloscope (or from Agilent .bin waveform files when running under debug mode only).
- initialize the oscilloscope settings to acquire test waveform data (Scale, Offset, Trigger, Memory depth, etc.).
- acquire the oscilloscope sample waveform data (re-iterate to capture at least 1M UI).
- perform the receiver compliance test function using the SigTest DLL.
- get the compliance test results from SigTest DLL.
- find and update the worst case test result values.
- calculate the Eye-Width and Differential Peak Output values. These values are used as the final test results in the Eye-Width test and the Differential Peak Output Voltage test.
- report the test results to ATE Framework.
- set the flags to indicate that the custom step has been called in the current test trial.

5. Report the measurement results.
6. Compare the measured RJ_rms value to the compliance test limits.

Measurement Algorithm

This is a timing measurement in PCI Express 2 that requires separation of the high frequency jitter on the transmitter signal.

The Receiver margining leverages LF(low frequency) / HF(high frequency) jitter separation methodology employed for the transmitter.

There are 2 different test IDs for the Receiver RMS Random Jitter Test as follow. The test procedure is the same for these tests with the exception of the template files used for the Data Clocked architecture and for the Common Refclk architecture.

a. Rx, Data Clocked Architecture RMS Random Jitter (PCIE 2.0): ID# 2282
b. Rx, Common Refclk Architecture RMS Random Jitter (PCIE 2.0): ID# 2284

Test References

The measured Random Jitter value for the test signal shall be within the conformance limit of ($T_{RX-TJ-CC}$ - $T_{RX-DJ-DD-CC}$) or ($T_{RX-TJ-CC}$ - $T_{RX-DJ-DD-DC}$) with reference to table 4-12 of the PCIE Base Specifications v2.0.

Rx, Maximum Deterministic Jitter

Test ID #:

2292 - Data Clocked Architecture

2294 - Common Refclk Architecture

Test Definition Notes from the Base Specification

Table 169 Peak Differential Output Voltage from Table 4-12 of the Base Specification: 2.5 and 5.0 GT/s Receiver Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$V_{RX-DJ-DD-CC}$	Max Rx inherent deterministic timing error	N/A	0.30 (max)	UI	Max Rx inherent deterministic timing error for common Refclk Rx architecture. See below note.
$V_{RX-DJ-DD-DC}$	Max Rx inherent deterministic timing error	N/A	0.24 (max)	UI	Max Rx inherent deterministic timing error for data clocked Rx architecture. See below note.

NOTE: The four inherent timing error parameters are defined for the convenience of Rx designers, and they are measured during Receiver tolerancing.

Test Procedure

1 Set the probe point to RX_2_0 for Data Clocked; or RX_CC_2_0 for Common Refclk.

2 Perform PreTest function (Utils.xml)

- construct extended FW test steps (e.g. CUST_GetMeasStatsStep, CUST_CancelChecker, etc.).

3 Perform the input signal scaling for display optimization and check the signal characteristics.

- This portion is only done if any of the following item changes:
    - probe point (e.g. TX, RX, etc.).
    - the user selectable signal source on the GUI configuration page.

    - the de-embed value on the GUI configuration page.
    - the lane number on the GUI configuration page.
- consist of probe external scaling to cater for the signal de-embed option.
- vertical auto-scaling of the input signal.
- initialize the FUNC2 as differential source.
- verify if the triggers exist
- verify that the minimum signal pulse width is within 1 UI range (for NON-RefClk test ONLY).
- verify that the maximum signal pulse width is within 5 UI range (for NON-RefClk test ONLY).

4 Perform actual compliance testing using the SigTest DLL (CUST_SigTestDLL_RxDataClkTest or CUST_SigTestDLL_RxCommonClkTest)

- check if the custom test step has been called in the current trial. This custom test step is designed to execute once per test trial.
- check if the required template file exist. The default template file is as follow.
    - Data Clocked architecture: "RX_DC_CON.dat" (modified from the SigTest Add-In Card template file).
    - Common Refclk architecture: "RX_CC_CON.dat" (modified from the SigTest System Board template file).
- get the framework configuration variables of interest.
- create plot data directory if it does not exist.
- get the input test waveform data from the oscilloscope (or from Agilent .bin waveform files when running under debug mode only).
- initialize the oscilloscope settings to acquire test waveform data (Scale, Offset, Trigger, Memory depth, etc.).
- acquire the oscilloscope sample waveform data (re-iterate to capture at least 1M UI).
- perform the receiver compliance test function using the SigTest DLL.
- get the compliance test results from SigTest DLL.
- find and update the worst case test result values.
- calculate the Eye-Width and Differential Peak Output values. These values are used as the final test results in the Eye-Width test and the Differential Peak Output Voltage test.
- report the test results to ATE Framework.
- set the flags to indicate that the custom step has been called in the current test trial.

5 Report the measurement results.

6 Compare the measured DJ_dd value to the compliance test limits.

Measurement Algorithm

This is a timing measurement in PCI Express 2 that requires separation of the high frequency jitter on the transmitter signal.

The Receiver margining leverages LF(low frequency) / HF(high frequency) jitter separation methodology employed for the transmitter.

There are 2 different test IDs for the Receiver Maximum Deterministic Jitter Test as follow. The test procedure is the same for these tests with the exception of the template files used for the Data Clocked architecture and for the Common Refclk architecture.

a Rx, Data Clocked Architecture Maximum Deterministic Jitter (PCIE 2.0): ID# 2292

b Rx, Common Refclk Architecture Maximum Deterministic Jitter (PCIE 2.0): ID# 2294

Test References

Table 4-12, PCI Express Base Specification v2.0.

Rx, Total Jitter at BER-12

Test ID #:

2296 - Data Clocked Architecture

2298 - Common Refclk Architecture

Test Definition Notes from the Base Specification

Table 170 From Table 4-12 of the Base Specification: 2.5 and 5.0 GT/s Receiver Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$V_{RX-TJ-CC}$	Max Rx inherent timing error	N/A	0.40 (max)	UI	Max Rx inherent total timing error for common Refclk Rx architecture. See below note.
$V_{RX-TJ-DC}$	Max Rx inherent timing error	N/A	034 (max)	UI	Max Rx inherent total timing error for data clocked Rx architecture. See below note.

NOTE: The four inherent timing error parameters are defined for the convenience of Rx designers, and they are measured during Receiver tolerancing.

Test Procedure

1 Set the probe point to RX_2_0 for Data Clocked; or RX_CC_2_0 for Common Refclk.

2 Perform PreTest function (Utils.xml)

- construct extended FW test steps (e.g. CUST_GetMeasStatsStep, CUST_CancelChecker, etc.).

3 Perform the input signal scaling for display optimization and check the signal characteristics.

- This portion is only done if any of the following item changes:
    - probe point (e.g. TX, RX, etc.).
    - the user selectable signal source on the GUI configuration page.
    - the de-embed value on the GUI configuration page.
    - the lane number on the GUI configuration page.
- consist of probe external scaling to cater for the signal de-embed option.
- vertical auto-scaling of the input signal.
- initialize the FUNC2 as differential source.
- verify if the triggers exist
- verify that the minimum signal pulse width is within 1 UI range (for NON-RefClk test ONLY).
- verify that the maximum signal pulse width is within 5 UI range (for NON-RefClk test ONLY).

4 Perform actual compliance testing using the SigTest DLL (CUST_SigTestDLL_RxDataClkTest or CUST_SigTestDLL_RxCommonClkTest)

- check if the custom test step has been called in the current trial. This custom test step is designed to execute once per test trial.
- check if the required template file exist. The default template file is as follow.
    - Data Clocked architecture: "RX_DC_CON.dat" (modified from the SigTest Add-In Card template file).
    - Common Refclk architecture: "RX_CC_CON.dat" (modified from the SigTest System Board template file).
- get the framework configuration variables of interest.
- create plot data directory if it does not exist.

- get the input test waveform data from the oscilloscope (or from Agilent .bin waveform files when running under debug mode only).
- initialize the oscilloscope settings to acquire test waveform data (Scale, Offset, Trigger, Memory depth, etc.).
- acquire the oscilloscope sample waveform data (re-iterate to capture at least 1M UI).
- perform the receiver compliance test function using the SigTest DLL.
- get the compliance test results from SigTest DLL.
- find and update the worst case test result values.
- calculate the Eye-Width and Differential Peak Output values. These values are used as the final test results in the Eye-Width test and the Differential Peak Output Voltage test.
- report the test results to ATE Framework.
- set the flags to indicate that the custom step has been called in the current test trial.

5 Report the measurement results.

6 Compare the measured Total Jitter at BER-12 value to the compliance test limits.

Measurement Algorithm

This is a timing measurement in PCI Express 2 that requires separation of the high frequency jitter on the transmitter signal.

The Receiver margining leverages LF(low frequency) / HF(high frequency) jitter separation methodology employed for the transmitter.

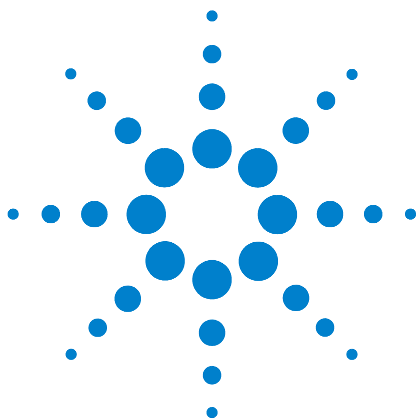
There are 2 different test IDs for the Receiver Maximum Deterministic Jitter Test as follow. The test procedure is the same for these tests with the exception of the template files used for the Data Clocked architecture and for the Common Refclk architecture.

a Rx, Data Clocked Total Jitter at BER-12 (PCIE 2.0): ID# 2296

b Rx, Data Clocked Total Jitter at BER-12 (PCIE 2.0): ID# 2298

Test References

Table 4-12, PCI Express Base Specification v2.0.



18
Add-In Card (Tx) Tests, 5.0 GT/s, PCI-E 2.0

Probing the Link for Add-In Card Compliance 302
Running Add-In Card Tests 305

This section provides the Methods of Implementation (MOIs) for Add-In Card (Tx) 5.0 GT/s tests of PCI-E 2.0 using an Agilent 80000B or 90000A series Infiniium oscilloscope, 1169A probes, and the PCI Express Automated Test Application.

Probing the Link for Add-In Card Compliance

Connecting the Compliance Base Board for Add-in Card Testing

There are multiple pairs of SMP connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1 With the Add-in card fixture power supply powered off, connect the power supply connector to the Add-in card test fixture, and connect the device under test add-in card to the by-16 connector slot.

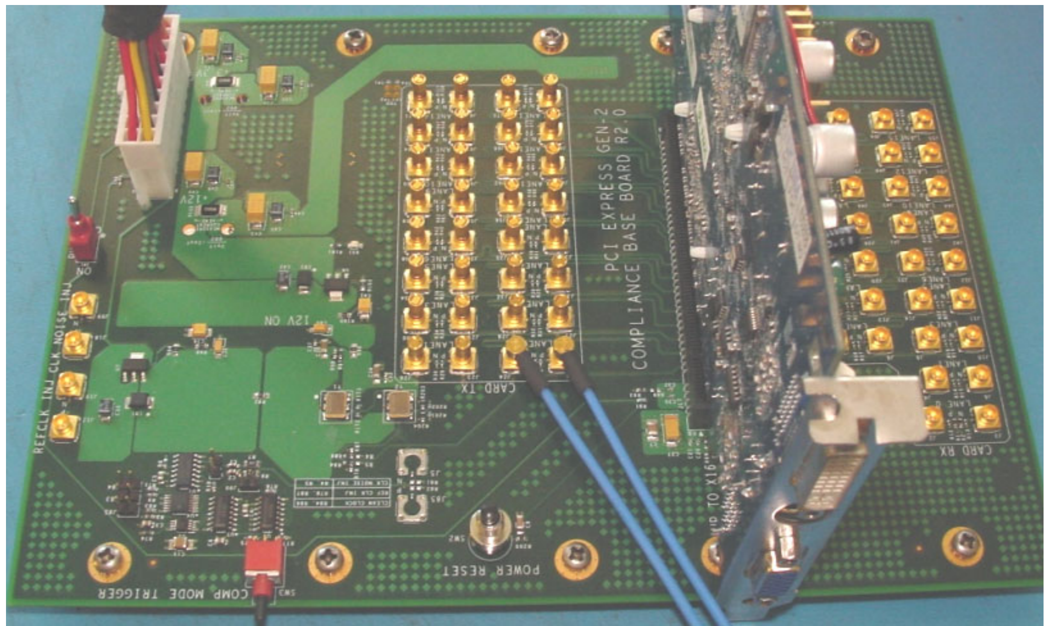


Figure 89 Compliance Base Board (CBB) Add-in Card Fixture

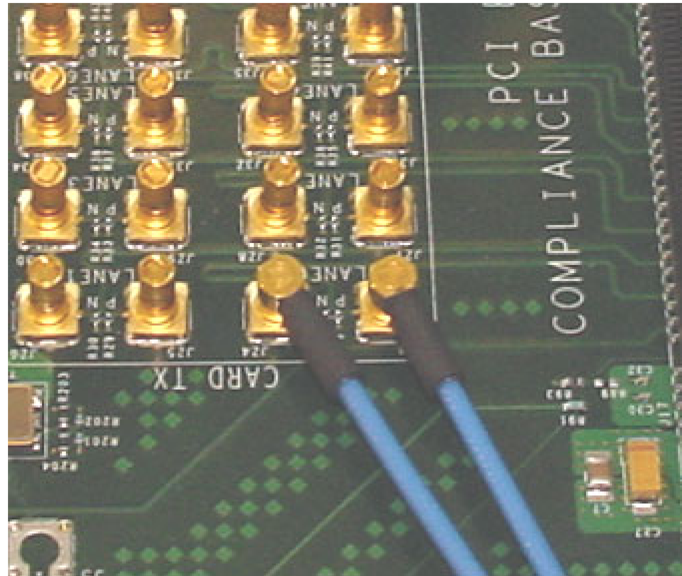


Figure 90 Compliance Base Board (CBB) 2.0 SMP Probing Option

2 Provide the proper Compliance Test Pattern by clicking the toggle switch until you reach the desired mode. The available options are 2.5 GHz at -3.5 dB de-emphasis mode, 5.0 GHz at -3.5 dB and 5.0 GHz at 6.0 dB.

3 Connect cables up as follows:

   a Digital Storage Oscilloscope channel 1 to the D+ (where Lane 1 is under test in this example shown in Figure 90 above).

   b Digital Storage Oscilloscope channel 3 to the D- (where Lane 1 is under test in this example shown in Figure 90 above).

When SMP probing and two channels are used, channel-to-channel deskew is required (see “Channel-to-Channel De-skew" on page 386).

Not all lanes have SMP probing options. For signal quality testing of the remaining lanes you will need to use a high bandwidth differential or single ended probes. For more information on the probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 392.

When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the probe amplifier.

4 Connect adequate load to the power supply to assure it is regulating and turned on. Generally, one IDE hard drive will provide adequate load.

5 Turn on the power supply. DS1 LED (located near the ATX power supply connector) should turn on. If the LED is on, but the power supply does not turn on, check that the jumper J7 is installed between J7-1 and J7-2.

Running Add-In Card Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 22. Then, when selecting tests, navigate to the "Add-In Card (Tx) Tests" group.

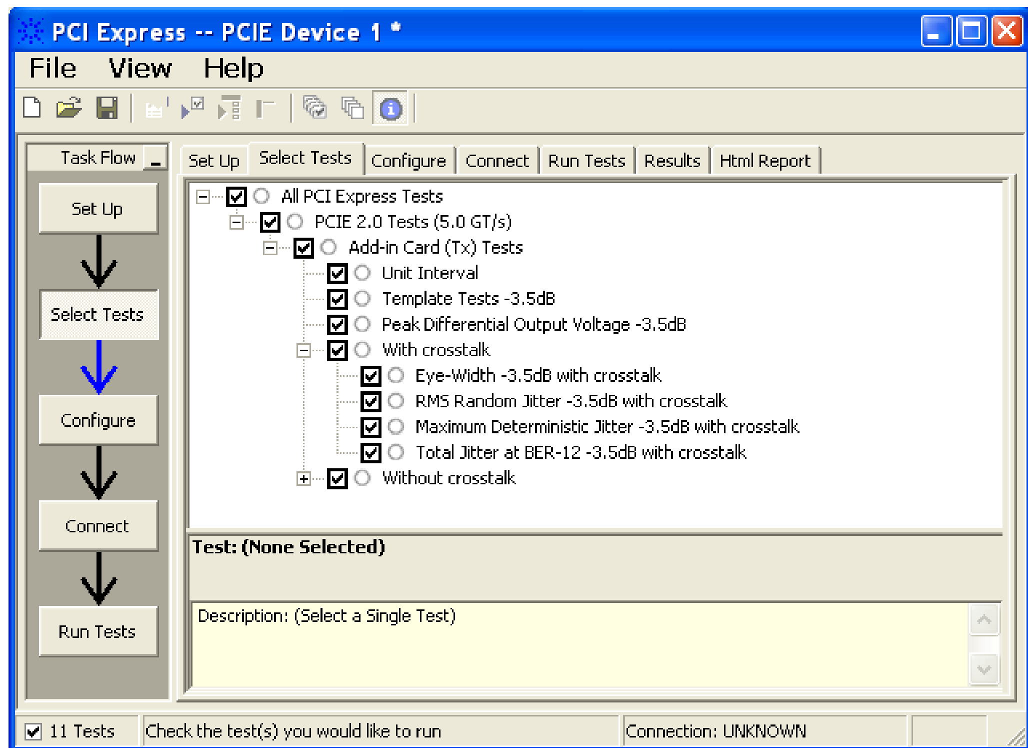


Figure 91 Selecting Add-In Card (Tx) Tests

Add-In Card Tx, Unit Interval

Test ID #:

2300

Test Definition Notes from the Specification

Table 171 Unit Interval from Table 4-9 of the Base Specification: 2.5 and 5.0 GT/s Transmitter Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
UI	Unit Interval	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)	ps	The specified UI is equivalent to a tolerance of ±300 ppm for each Refclk source. Period does not account for SSC caused variations. See below note.

NOTE: SSC permits a +0, -5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33 kHz.

Test Procedure

1 Set the probe point to ADDIN_TX_2_0
2 Perform the PreTest function (Utils.xml)
- construct extended FW test steps (eg. CUST_GetMeasStatsStep, CUST_CancelChecker, etc).

3 Perform the input signal scaling for display optimization and check the signal characteristics.
- This portion is only done if any of the following item changes:
  - probe point (eg. TX, RX, etc).
  - the user selectable signal source on the GUI configuration page.
  - the de-embed value on the GUI configuration page.
  - the lane number on the GUI configuration page.
- consist of probe external scaling to cater for signal de-embed option.
- vertical auto-scaling of input signal.
- initialize FUNC2 as differential source.
- verify if the triggers exist.
- verify that the minimum signal pulse width is within 1 UI range (for NON-RefClk test ONLY).
- verify that the maximum signal pulse width is within 5 UI range (for NON-RefClk test ONLY).

4 Setup labels and grid display settings on the oscilloscope (SetupUI.cmd).
5 Sets the scale and offset of the input channels to their optimum values.
6 Sets the Sample Rate, Enhanced BW, and Memory Depth to the values requested on the configuration page of the GUI.

7 Sets the trigger source and trigger level defined by the user on the configuration page of the GUI.
8 Fit and display all the data sample data on the screen.
9 Use "Unit Interval" measurement on the oscilloscope (EZJit option) and jitter TREND function.
10 Use marker to indicate the upper and lower limit on the FUNC3 (Trend data of UI measurements).
11 Measure UI_max, UI_min and UI_average from FUNC3.
12 Report the measurement results.

Measurement Algorithm

A recovered TX UI is calculated over 3500 consecutive unit intervals of a sample data as the mean unit interval over the clock recovery window.

TX UI(p) = Mean(UI(n))

Where:

n is the index of UI in the clock recovery window.

p indicates the pth 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

Test References

Table 4-9, Section 4.3.3.5, PCI Express Base Specification v2.0.

NOTE The UI measurement is not required at this point. It is provided as an informative test only.

NOTE The TX UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another TX UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The mean TX UI is reported.

Add-In Card Tx, Template Tests

Test ID #:

2316 (-3.5 dB)

2318 (-6.0 dB)

Test Definition Notes from the Specification

Table 172 Add-in Card Transmitter Path Compliance Eye Requirements from Table 4-8 of the Base Specification: 5.0 GT/s at 3.5 dB De-emphasis

Parameter	Min	Max	Unit	Comments
V_{TXA}	380	1200	mV	Notes 1, 2, 4
V_{TXA_d}	380	1200	mV	Notes 1, 2, 4
T_{TXA} (with crosstalk)	123		ps	Notes 1, 3, 4
T_{TXA} (without crosstalk)	126		ps	

Table 173 Add-in Card Transmitter Path Compliance Eye Requirements from Table 4-10 of the Base Specification: 5.0 GT/s at 6.0 dB De-emphasis

Parameter	Min	Max	Unit	Comments
V_{TXA}	306	1200	mV	Notes 1, 2, 4
V_{TXA_d}	260	1200	mV	Notes 1, 2, 4
T_{TXA} (with crosstalk)	123		ps	Notes 1, 3, 4
T_{TXA} (without crosstalk)	126		ps	

NOTES 1: An ideal reference clock without jitter is assumed for this specification. All links are assumed active while generating this eye diagram. The eye diagram requires that CMM pattern *(PCI Express Base Specification, Revision 2.0, Section 4.2.8)* is being transmitted during the test.

NOTES 2: Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.

NOTES 3: T_{TXA} is the minimum eye width. The recommended sample size for this measurement is at least 10^5 UI. This calculated eye width at BER 10^{-12} must not exceed T_{TXA}. If the add-in card board uses non-interleaved routing, then crosstalk will be present in the measurement data. If the add-in card board uses interleaved routing, then crosstalk will not be present and an adjusted minimum eye width is used.

NOTES 4: The values in Table 173 are referenced to an ideal 100 Ω differential load at the end of an isolated 3-inch long 85 Ω differential trace behind a standard PCI Express connector. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PHY Electrical Test Considerations for PCI Express Architecture* document.

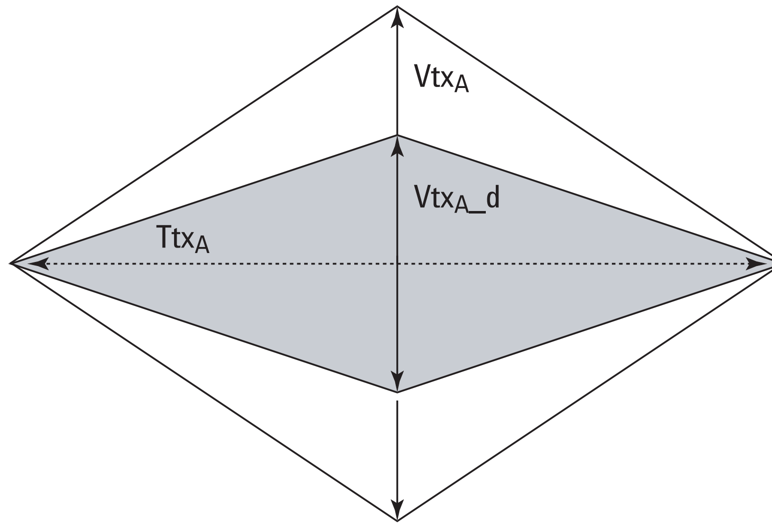


Figure 92 Add-In Card Tx Compliance Eye Diagram

Test Procedure

1 Set the probe point to ADDIN_TX_2_0.

2 Perform the PreTest function (Utils.xml)

- construct extended FW test steps (eg. CUST_GetMeasStatsStep, CUST_CancelChecker, etc).

3 Perform the input signal scaling for display optimization and check the signal characteristics.

- This portion is only done if any of the following item changes:
  - probe point (eg. TX, RX, etc).
  - the user selectable signal source on the GUI configuration page.
  - the de-embed value on the GUI configuration page.
  - the lane number on the GUI configuration page.
- consist of probe external scaling to cater for signal de-embed option.
- vertical auto-scaling of input signal.
- initialize the FUNC2 as differential source.
- verify if the triggers exist.
- verify that the minimum signal pulse width is within 1 UI range (for NON-RefClk test ONLY).
- verify that the maximum signal pulse width is within 5 UI range (for NON-RefClk test ONLY).

4 Perform the actual compliance testing using the SigTest DLL (CUST_SigTestDLL_AddInCardTest).

- check if the custom test step has been called in the current trial. This custom test step is designed to execute once per test trial.
- check if the required template file exist. The default template file is “TX_ADD_CON_3.5DB.dat”.
- get the framework configuration variables of interest.
- create plot data directory if it does not exist.
- get the input test waveform data from the oscilloscope (or from Agilent. bin waveform files when running under debug mode only).
- initialize the oscilloscope settings to acquire test waveform data (Scale, Offset, Trigger, Memory depth, etc.).
- acquire the oscilloscope sample waveform data (re-iterate to capture at least 1M UI).
- perform the Add-In Card compliance test function using the SigTest DLL.
- get the compliance test results from SigTest DLL.
- find and update the worst case test result values.
- calculate the Eye-Width and Differential Peak Output values. These values are used as the final test results in the Eye-Width test and the Differential Peak Output Voltage test.
- report the test results to ATE Framework.
- set the flags to indicate that the custom step has been called in the current test trial.

5 Report the measurement results.

6 Display the eye diagrams (transition and non-transition) generated using the SigTest DLL plot data.

7 Check for mask failures in both transition and non-transition eye diagrams. Test will fail if total failures are not equal to zero.

Measurement Algorithm

Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye requirements specified in table 4-8 of section 4.7.2 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in figure 4-7.

All Links are assumed active while generating this eye diagram. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}).

There are 2 different test IDs for the Add-in Card Template Tests as follow. The test procedure is the same for these tests with the exception of the template files used for the -3.5dB and the-6.0dB.

a. Add-in Card Tx, Template Tests -3.5dB (PCIE 2.0) : ID# 2316
b. Add-in Card Tx, Template Tests -6.0dB (PCIE 2.0) : ID# 2318

Test References

Table 4-8 and Table 4-10, Section 4.7.2, PCI Express Base Specification v2.0.

The number of mask violation shall be 0.

Add-In Card Tx, Peak Differential Output Voltage

Test ID #:

2346 (-3.5 dB)

2348 (-6.0 dB)

Test Definition Notes from the Specification

Table 174 Add-in Card Transmitter Path Compliance Eye Requirements from Table 4-8 of the Base Specification: 5.0 GT/s at 3.5 dB De-emphasis

Parameter	Min	Max	Unit	Comments
V_{TXA}	380	1200	mV	Notes 1, 2, 3
V_{TXA_d}	380	1200	mV	Notes 1, 2, 3

Table 175 Add-in Card Transmitter Path Compliance Eye Requirements from Table 4-10 of the Base Specification: 5.0 GT/s at 6.0 dB De-emphasis

Parameter	Min	Max	Unit	Comments
V_{TXA}	306	1200	mV	Notes 1, 2, 3
V_{TXA_d}	260	1200	mV	Notes 1, 2, 3

NOTES 1: An ideal reference clock without jitter is assumed for this specification. All links are assumed active while generating this eye diagram. The eye diagram requires that CMM pattern *(PCI Express Base Specification, Revision 2.0, Section 4.2.8)* is being transmitted during the test.

NOTES 2: Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.

NOTES 3: The values in Table 175 are referenced to an ideal 100 Ω differential load at the end of an isolated 3-inch long 85 Ω differential trace behind a standard PCI Express connector. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PHY Electrical Test Considerations for PCI Express Architecture* document.

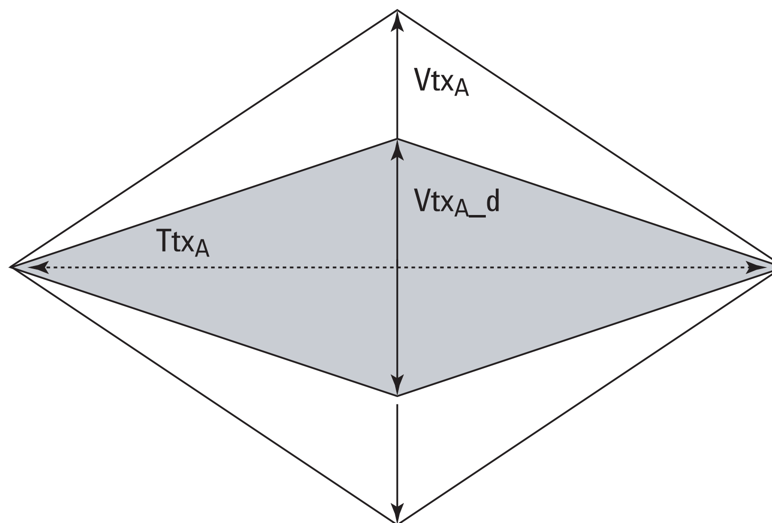


Figure 93 Add-In Card Tx Compliance Eye Diagram

Test Procedure

1 Set the probe point to ADDIN_TX_2_0.
2 Perform the PreTest function (Utils.xml)
- construct extended FW test steps (eg. CUST_GetMeasStatsStep, CUST_CancelChecker, etc).

3 Perform the input signal scaling for display optimization and check the signal characteristics.
- This portion is only done if any of the following item changes:
  - probe point (eg. TX, RX, etc).
  - the user selectable signal source on the GUI configuration page.
  - the de-embed value on the GUI configuration page.
  - the lane number on the GUI configuration page.
- consist of probe external scaling to cater for signal de-embed option.

- vertical auto-scaling of input signal.
- initialize the FUNC2 as differential source.
- verify if the triggers exist.
- verify that the minimum signal pulse width is within 1 UI range (for NON-RefClk test ONLY).
- verify that the maximum signal pulse width is within 5 UI range (for NON-RefClk test ONLY).

4 Perform the actual compliance testing using the SigTest DLL (CUST_SigTestDLL_AddInCardTest).

- check if the custom test step has been called in the current trial. This custom test step is designed to execute once per test trial.
- check if the required template file exist. The default template file is “TX_ADD_CON_3.5DB.dat”.
- get the framework configuration variables of interest.
- create plot data directory if it does not exist.
- get the input test waveform data from the oscilloscope (or from Agilent. bin waveform files when running under debug mode only).
- initialize the oscilloscope settings to acquire test waveform data (Scale, Offset, Trigger, Memory depth, etc.).
- acquire the oscilloscope sample waveform data (re-iterate to capture at least 1M UI).
- perform the Add-In Card compliance test function using the SigTest DLL.
- get the compliance test results from SigTest DLL.
- find and update the worst case test result values.
- calculate the Eye-Width and Differential Peak Output values. These values are used as the final test results in the Eye-Width test and the Differential Peak Output Voltage test.
- report the test results to ATE Framework.
- set the flags to indicate that the custom step has been called in the current trial.

5 Report the measurement results.

6 Compare the measured peak voltage (WorstValue) value to the compliance test limits.

Measurement Algorithm

The Differential Peak Voltage measurement returns two times the larger of the Min or Max statistic of the differential voltage waveform.

$V_{TX-DIFF-p-p} = 2 * Max (Max(V_{DIFF(i)}), Min(V_{DIFF(i)}))$

Where:

i is the index of all waveform values.

V_{DIFF} is the Differential Voltage signal.

There are 2 different test IDs for the Add-in Card Peak Differential Output Voltage Tests as follow. The test procedure is the same for these tests with the exception of the compliance test limits used for the -3.5 dB and the-6.0 dB.

a Add-in Card Tx, Peak Differential Output Voltage Tests -3.5 dB (PCIE 2.0) : ID# 2346

b Add-in Card Tx, Peak Differential Output Voltage Tests -6.0 dB (PCIE 2.0) : ID# 2348

Test References

Table 4-8 and Table 4-10, Section 4.7.2, PCI Express Base Specification v2.0.

The $V_{TX-DIFF-p-p}$ value is within the conformance range limits:

(380mV <= $V_{TX-DIFF-p-p}$ <= 1.2V) for -3.5 dB signaling

(306mV <= $V_{TX-DIFF-p-p}$ <= 1.2V) for -6.0 dB signaling

Add-In Card Tx, Eye-Width

Test ID #:

2336 (-3.5 dB with crosstalk)

2337 (-3.5 dB without crosstalk)

2338 (-6.0 dB with crosstalk)

2339 (-6.0 dB without crosstalk)

Test Definition Notes from the Specification

Table 176 Add-in Card Transmitter Path Compliance Eye Requirements from Table 4-8 of the Base Specification: 5.0 GT/s at 3.5 dB De-emphasis

Parameter	Min	Max	Unit	Comments
V_{TXA} (with crosstalk)	123		ps	Notes 1, 2, 3
V_{TXA} (without crosstalk)	126		ps	

Table 177 Add-in Card Transmitter Path Compliance Eye Requirements from Table 4-10 of the Base Specification: 5.0 GT/s at 6.0 dB De-emphasis

Parameter	Min	Max	Unit	Comments
V_{TXA} (with crosstalk)	123		ps	Notes 1, 2, 3
V_{TXA} (without crosstalk)	126		ps	

NOTES 1: An ideal reference clock without jitter is assumed for this specification. All links are assumed active while generating this eye diagram. The eye diagram requires that CMM pattern *(PCI Express Base Specification, Revision 2.0, Section 4.2.8)* is being transmitted during the test.

NOTES 2: T_{TXA} is the minimum eye width. The recommended sample size for this measurement is at least 10^5 UI. This calculated eye width at BER 10^{-12} must not exceed T_{TXA}. If the add-in card board uses non-interleaved routing, then crosstalk will be present in the measurement data. If the add-in card board uses interleaved routing, then crosstalk will not be present and an adjusted minimum eye width is used.

NOTES 3: The values in Table 177 are referenced to an ideal 100 Ω differential load at the end of an isolated 3-inch long 85 Ω differential trace behind a standard PCI Express connector. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PHY Electrical Test Considerations for PCI Express Architecture* document.

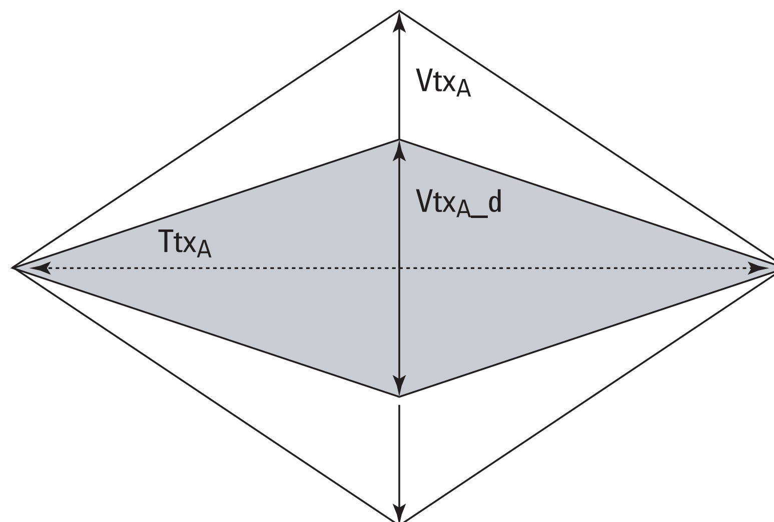


Figure 94 Add-In Card Tx Compliance Eye Diagram

Test Procedure

1 Set the probe point to ADDIN_TX_2_0.
2 Perform the PreTest function (Utils.xml)

- construct extended FW test steps (eg. CUST_GetMeasStatsStep, CUST_CancelChecker, etc).

3 Perform the input signal scaling for display optimization and check the signal characteristics.

- This portion is only done if any of the following item changes:
  - probe point (eg. TX, RX, etc).
  - the user selectable signal source on the GUI configuration page.
  - the de-embed value on the GUI configuration page.
  - the lane number on the GUI configuration page.
- consist of probe external scaling to cater for signal de-embed option.
- vertical auto-scaling of input signal.
- initialize the FUNC2 as differential source.
- verify if the triggers exist.
- verify that the minimum signal pulse width is within 1 UI range (for NON-RefClk test ONLY).
- verify that the maximum signal pulse width is within 5 UI range (for NON-RefClk test ONLY).

4 Perform the actual compliance testing using the SigTest DLL (CUST_SigTestDLL_AddInCardTest).

- check if the custom test step has been called in the current trial. This custom test step is designed to execute once per test trial.
- check if the required template file exist. The default template file is “TX_ADD_CON_3.5DB.dat”.
- get the framework configuration variables of interest.
- create plot data directory if it does not exist.
- get the input test waveform data from the oscilloscope (or from Agilent. bin waveform files when running under debug mode only).
- initialize the oscilloscope settings to acquire test waveform data (Scale, Offset, Trigger, Memory depth, etc.).
- acquire the oscilloscope sample waveform data (re-iterate to capture at least 1M UI).
- perform the Add-In Card compliance test function using the SigTest DLL.
- get the compliance test results from SigTest DLL.
- find and update the worst case test result values.

- calculate the Eye-Width and Differential Peak Output values. These values are used as the final test results in the Eye-Width test and the Differential Peak Output Voltage test.
- report the test results to ATE Framework.
- set the flags to indicate that the custom step has been called in the current test trial.

5 Report the measurement results.

6 Compare the measured Eye-Width value to the compliance test limits.

Measurement Algorithm

This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [total jitter at BER-12]. This parameter is measured with the equivalent of a zero jitter reference clock.

There are 4 different test IDs for the Add-in Card Eye Width Tests as follow. The test procedure is the same for these tests with the exception of the template files and compliance test limits for the -3.5 dB and the-6.0 dB (both with and without crosstalk).

a Add-in Card Tx, Eye-Width -3.5 dB with crosstalk (PCIE 2.0): ID# 2336

b Add-in Card Tx, Eye-Width -3.5 dB without crosstalk (PCIE 2.0): ID# 2337

c Add-in Card Tx, Eye-Width -6.0 dB with crosstalk (PCIE 2.0): ID# 2338

d Add-in Card Tx, Eye-Width -6.0 dB without crosstalk (PCIE 2.0): ID# 2339

Test References

Table 4-8 and Table 4-10, Section 4.7.2, PCI Express Base Specification v2.0.

The measured Eye Width value shall be greater than 126 ps (without crosstalk) or 123 ps (with crosstalk).

Add-In Card Tx, RMS Random Jitter

Test ID #:

2382 (-3.5 dB with crosstalk)

2383 (-3.5 dB without crosstalk)

2384 (-6.0 dB with crosstalk)

2385 (-6.0 dB without crosstalk)

Test Definition Notes from the Specification

Table 178 Add-in Card Jitter Requirement for 5 GT/s Signaling at 3.5 dB De-emphasis: from Table 4-9 of the Base Specification

Parameter	Max Dj (ps)	Tj at BER 10^{-12} (ps)
With crosstalk	57	77
Without crosstalk	54	74

Table 179 Add-in Card Jitter Requirement for 5 GT/s Signaling at 6.0 dB De-emphasis: from Table 4-11 of the Base Specification

Parameter	Max Dj (ps)	Tj at BER 10^{-12} (ps)
With crosstalk	57	77
Without crosstalk	54	74

NOTE The RMS RJ range for this test is not specified in the CEM specification document. It is provided as an informative test only.

Test Procedure

1 Set the probe point to ADDIN_TX_2_0.

2 Perform the PreTest function (Utils.xml)

- construct extended FW test steps (eg. CUST_GetMeasStatsStep, CUST_CancelChecker, etc).

3 Perform the input signal scaling for display optimization and check the signal characteristics.

- This portion is only done if any of the following item changes:
  - probe point (eg. TX, RX, etc).
  - the user selectable signal source on the GUI configuration page.
  - the de-embed value on the GUI configuration page.
  - the lane number on the GUI configuration page.
- consist of probe external scaling to cater for signal de-embed option.
- vertical auto-scaling of input signal.
- initialize the FUNC2 as differential source.
- verify if the triggers exist.
- verify that the minimum signal pulse width is within 1 UI range (for NON-RefClk test ONLY).

- verify that the maximum signal pulse width is within 5 UI range (for NON-RefClk test ONLY).

4 Perform the actual compliance testing using the SigTest DLL (CUST_SigTestDLL_AddInCardTest).

- check if the custom test step has been called in the current trial. This custom test step is designed to execute once per test trial.
- check if the required template file exist. The default template file is "TX_ADD_CON_3.5DB.dat".
- get the framework configuration variables of interest.
- create plot data directory if it does not exist.
- get the input test waveform data from the oscilloscope (or from Agilent. bin waveform files when running under debug mode only).
- initialize the oscilloscope settings to acquire test waveform data (Scale, Offset, Trigger, Memory depth, etc.).
- acquire the oscilloscope sample waveform data (re-iterate to capture at least 1M UI).
- perform the Add-In Card compliance test function using the SigTest DLL.
- get the compliance test results from SigTest DLL.
- find and update the worst case test result values.
- calculate the Eye-Width and Differential Peak Output values. These values are used as the final test results in the Eye-Width test and the Differential Peak Output Voltage test.
- report the test results to ATE Framework.
- set the flags to indicate that the custom step has been called in the current test trial.

5 Report the measurement results.

6 Compare the measured Random Jitter value to the compliance test limits.

Measurement Algorithm

This is a timing measurement in PCI Express Gen2 that requires separation of the high frequency jitter on the transmitter signal.

The transmitter is tested with a low jitter reference clock (clean clock). However, the reference clock may still have some low frequency wander. Besides that, the transmitter itself may have low frequency wander from

VDD (supply voltage), temperature and other affects. In order to avoid this increasing observed transmitter jitter, jitter on the recovered clock is separated into different bands and measured.

1 High frequency jitter (above 1.5 MHz) that is not tracked by the receiver and therefore reduces the transmitter eye width.
2 Low frequency jitter (10kHz - 1.5MHz) that is mostly tracked by the receiver and used as part of the receiver testing.
3 Jitter below 10 kHz that is considered wander or drift and are tracked by the receiver.

There are 4 different test IDs for the Add-in Card RMS Random Jitter Tests as follow. The test procedure is the same for these tests with the exception of the template files and compliance test limits for the -3.5 dB and the-6.0 dB (both with and without crosstalk).

- a Add-in Card Tx, RMS Random Jitter -3.5 dB with crosstalk (PCIE 2.0): ID# 2382
- b Add-in Card Tx, RMS Random Jitter -3.5 dB without crosstalk (PCIE 2.0): ID# 2383
- c Add-in Card Tx, RMS Random Jitter -6.0 dB with crosstalk (PCIE 2.0): ID# 2384
- d Add-in Card Tx, RMS Random Jitter -6.0 dB without crosstalk (PCIE 2.0): ID# 2385

Test References

Table 4-9 and Table 4-11, Section 4.7.2, PCI Express Base Specification v2.0.

The measured Random Jitter value for the test signal shall be within the conformance limit value of (TJ_{BER-12} - DJ_{Max}).

Add-In Card Tx, Maximum Deterministic Jitter

Test ID #:

2392 (-3.5 dB with crosstalk)

2393 (-3.5 dB without crosstalk)

2394 (-6.0 dB with crosstalk)

2395 (-6.0 dB without crosstalk)

Test Definition Notes from the Specification

Table 180 Add-in Card Jitter Requirement for 5 GT/s Signaling at 3.5 dB De-emphasis: from Table 4-9 of the Base Specification

Parameter	Max Dj (ps)
With crosstalk	57
Without crosstalk	54

Table 181 Add-in Card Jitter Requirement for 5 GT/s Signaling at 6.0 dB De-emphasis: from Table 4-11 of the Base Specification

Parameter	Max Dj (ps)
With crosstalk	57
Without crosstalk	54

Test Procedure

1 Set the probe point to ADDIN_TX_2_0.

2 Perform the PreTest function (Utils.xml)

- construct extended FW test steps (eg. CUST_GetMeasStatsStep, CUST_CancelChecker, etc).

3 Perform the input signal scaling for display optimization and check the signal characteristics.

- This portion is only done if any of the following item changes:
  - probe point (eg. TX, RX, etc).
  - the user selectable signal source on the GUI configuration page.
  - the de-embed value on the GUI configuration page.
  - the lane number on the GUI configuration page.
- consist of probe external scaling to cater for signal de-embed option.
- vertical auto-scaling of input signal.
- initialize the FUNC2 as differential source.
- verify if the triggers exist.
- verify that the minimum signal pulse width is within 1 UI range (for NON-RefClk test ONLY).
- verify that the maximum signal pulse width is within 5 UI range (for NON-RefClk test ONLY).

4 Perform the actual compliance testing using the SigTest DLL (CUST_SigTestDLL_AddInCardTest).

- check if the custom test step has been called in the current trial. This custom test step is designed to execute once per test trial.
- check if the required template file exist. The default template file is "TX_ADD_CON_3.5DB.dat".
- get the framework configuration variables of interest.
- create plot data directory if it does not exist.
- get the input test waveform data from the oscilloscope (or from Agilent. bin waveform files when running under debug mode only).
- initialize the oscilloscope settings to acquire test waveform data (Scale, Offset, Trigger, Memory depth, etc.).
- acquire the oscilloscope sample waveform data (re-iterate to capture at least 1M UI).
- perform the Add-In Card compliance test function using the SigTest DLL.
- get the compliance test results from SigTest DLL.
- find and update the worst case test result values.
- calculate the Eye-Width and Differential Peak Output values. These values are used as the final test results in the Eye-Width test and the Differential Peak Output Voltage test.
- report the test results to ATE Framework.
- set the flags to indicate that the custom step has been called in the current test trial.

5 Report the measurement results.

6 Compare the measured Deterministic Jitter value to the compliance test limits.

Measurement Algorithm

This is a timing measurement in PCI Express Gen2 that requires separation of the high frequency jitter on the transmitter signal.

The transmitter is tested with a low jitter reference clock (clean clock). However, the reference clock may still have some low frequency wander. Besides that, the transmitter itself may have low frequency wander from VDD (supply voltage), temperature and other affects. In order to avoid this increasing observed transmitter jitter, jitter on the recovered clock is separated into different bands and measured.

1. High frequency jitter (above 1.5 MHz) that is not tracked by the receiver and therefore reduces the transmitter eye width.
2. Low frequency jitter (10kHz - 1.5MHz) that is mostly tracked by the receiver and used as part of the receiver testing.

3 Jitter below 10 kHz that is considered wander or drift and are tracked by the receiver.

There are 4 different test IDs for the Add-in Card Maximum Jitter Tests as follow. The test procedure is the same for these tests with the exception of the template files and compliance test limits for the -3.5 dB and the-6.0 dB (both with and without crosstalk).

a Add-in Card Tx, Maximum Deterministic Jitter -3.5 dB with crosstalk (PCIE 2.0): ID# 2392

b Add-in Card Tx, Maximum Deterministic Jitter -3.5 dB without crosstalk (PCIE 2.0): ID# 2393

c Add-in Card Tx, Maximum Deterministic Jitter -6.0 dB with crosstalk (PCIE 2.0): ID# 2394

d Add-in Card Tx, Maximum Deterministic Jitter -6.0 dB without crosstalk (PCIE 2.0): ID# 2395

Test References

Table 4-9 and Table 4-11, Section 4.7.2, PCI Express Base Specification v2.0.

Add-In Card Tx, Total Jitter at BER-12

Test ID #:

2396 (-3.5 dB with crosstalk)

2397 (-3.5 dB without crosstalk)

2398 (-6.0 dB with crosstalk)

2399 (-6.0 dB without crosstalk)

Test Definition Notes from the Specification

Table 182 Add-in Card Jitter Requirement for 5 GT/s Signaling at 3.5 dB De-emphasis: from Table 4-9 of the Base Specification

Parameter	Max Dj (ps)
With crosstalk	77
Without crosstalk	74

Table 183 Add-in Card Jitter Requirement for 5 GT/s Signaling at 6.0 dB De-emphasis: from Table 4-11 of the Base Specification

Parameter	Max Dj (ps)
With crosstalk	77
Without crosstalk	74

Test Procedure

1 Set the probe point to ADDIN_TX_2_0.

2 Perform the PreTest function (Utils.xml)

- construct extended FW test steps (eg. CUST_GetMeasStatsStep, CUST_CancelChecker, etc).

3 Perform the input signal scaling for display optimization and check the signal characteristics.

- This portion is only done if any of the following item changes:
    - probe point (eg. TX, RX, etc).
    - the user selectable signal source on the GUI configuration page.
    - the de-embed value on the GUI configuration page.
    - the lane number on the GUI configuration page.
- consist of probe external scaling to cater for signal de-embed option.
- vertical auto-scaling of input signal.
- initialize the FUNC2 as differential source.
- verify if the triggers exist.
- verify that the minimum signal pulse width is within 1 UI range (for NON-RefClk test ONLY).
- verify that the maximum signal pulse width is within 5 UI range (for NON-RefClk test ONLY).

4 Perform the actual compliance testing using the SigTest DLL (CUST_SigTestDLL_AddInCardTest).

- check if the custom test step has been called in the current trial. This custom test step is designed to execute once per test trial.
- check if the required template file exist. The default template file is “TX_ADD_CON_3.5DB.dat”.
- get the framework configuration variables of interest.
- create plot data directory if it does not exist.
- get the input test waveform data from the oscilloscope (or from Agilent. bin waveform files when running under debug mode only).

- initialize the oscilloscope settings to acquire test waveform data (Scale, Offset, Trigger, Memory depth, etc.).
- acquire the oscilloscope sample waveform data (re-iterate to capture at least 1M UI).
- perform the Add-In Card compliance test function using the SigTest DLL.
- get the compliance test results from SigTest DLL.
- find and update the worst case test result values.
- calculate the Eye-Width and Differential Peak Output values. These values are used as the final test results in the Eye-Width test and the Differential Peak Output Voltage test.
- report the test results to ATE Framework.
- set the flags to indicate that the custom step has been called in the current test trial.

5 Report the measurement results.
6 Compare the measured Total Jitter at BER-12 value to the compliance test limits.

Measurement Algorithm

This is a timing measurement in PCI Express Gen2 that requires separation of the high frequency jitter on the transmitter signal.

The transmitter is tested with a low jitter reference clock (clean clock). However, the reference clock may still have some low frequency wander. Besides that, the transmitter itself may have low frequency wander from VDD (supply voltage), temperature and other affects. In order to avoid this increasing observed transmitter jitter, jitter on the recovered clock is separated into different bands and measured.

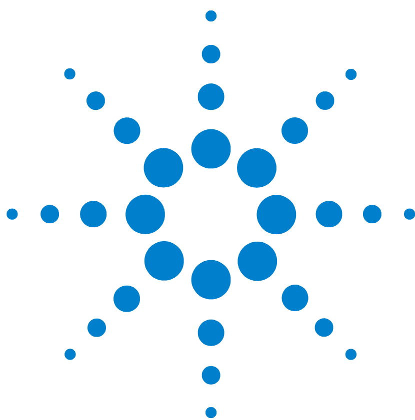
1. High frequency jitter (above 1.5 MHz) that is not tracked by the receiver and therefore reduces the transmitter eye width.
2. Low frequency jitter (10kHz - 1.5MHz) that is mostly tracked by the receiver and used as part of the receiver testing.
3. Jitter below 10 kHz that is considered wander or drift and are tracked by the receiver.

There are 4 different test IDs for the Add-in Card Total Jitter at BER-12 Tests as follow. The test procedure is the same for these tests with the exception of the template files and compliance test limits for the -3.5 dB and the-6.0 dB (both with and without crosstalk).

- **a** Add-in Card Tx, Total Jitter -3.5 dB with crosstalk (PCIE 2.0): ID# 2396
- **b** Add-in Card Tx, Total Jitter -3.5 dB without crosstalk (PCIE 2.0): ID# 2397
- **c** Add-in Card Tx, Total Jitter -6.0 dB with crosstalk (PCIE 2.0): ID# 2398
- **d** Add-in Card Tx, Total Jitter -6.0 dB without crosstalk (PCIE 2.0): ID# 2399

Test References

Table 4-9 and Table 4-11, Section 4.7.2, PCI Express Base Specification v2.0.



19
System Board (Tx) Tests, 5.0 GT/s, PCI-E 2.0

Probing the Link for System Board Compliance 327
Running System Board Tests 329

This section provides the Methods of Implementation (MOIs) for System Board (Tx) 5.0 GT/s tests of PCI-E 2.0 using an Agilent 80000B or 90000A series Infiniium oscilloscope, 1169A probes, and the PCI Express Automated Test Application.

Probing the Link for System Board Compliance

Connecting the Signal Quality Load Board for System/Motherboard Testing

There are multiple pairs of SMP connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1 With the system/motherboard powered off, connect the Compliance PCI Express Signal Quality Load Board into the connector under test. The are 2 types of PCI Express Signal Quality Load Board edge fingers combination available - x1 and x16 connectors, as well as x4 and x8 connectors.

   The PCI Express Signal Quality Load Board will cause a PCI Express 2.0 Base Specification System/motherboard to enter the compliance sub-state of the polling state. During this state the device under test will repeatedly send out the compliance pattern defined in the PCI Express Base Specification.

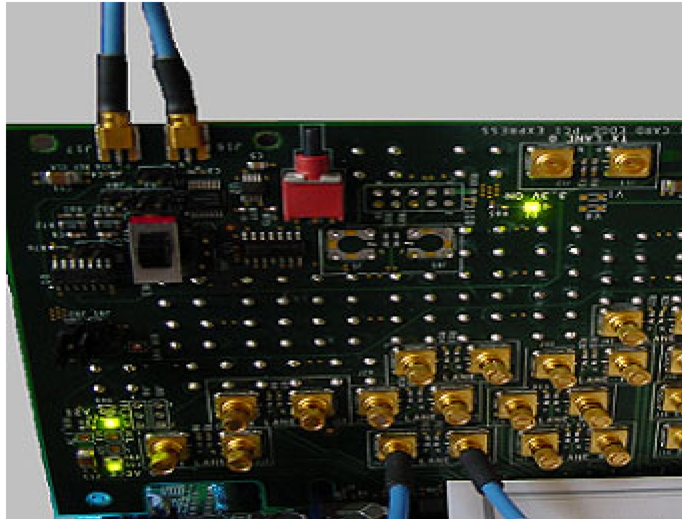


Figure 95 SMP Probing Option

2 Provide the proper Compliance Test Pattern by clicking the toggle switch until you reach the desired mode. The available options are 2.5 GHz at -3.5 dB de-emphasis mode, 5.0 GHz at -3.5 dB and 5.0 GHz at 6.0 dB.

3 Connect cables up as follows:

   a Digital Storage Oscilloscope channel 1 to Data and Channel 3 to Clock OR

   b Digital Storage Oscilloscope channel 2 to Data and Channel 4 to Clock.

   When SMP probing and two channels are used, channel-to-channel deskew is required (see "Channel-to-Channel De-skew" on page 386).

   Not all lanes have SMP probing options. For signal quality testing of the remaining lanes you will need to use a high bandwidth differential or single ended probes. For more information on the probe amplifiers and differential probe heads, see Appendix B, "InfiniiMax Probing Options," starting on page 392.

   When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the probe amplifier.

Running System Board Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 22. Then, when selecting tests, navigate to the "System Board (Tx) Tests" group.

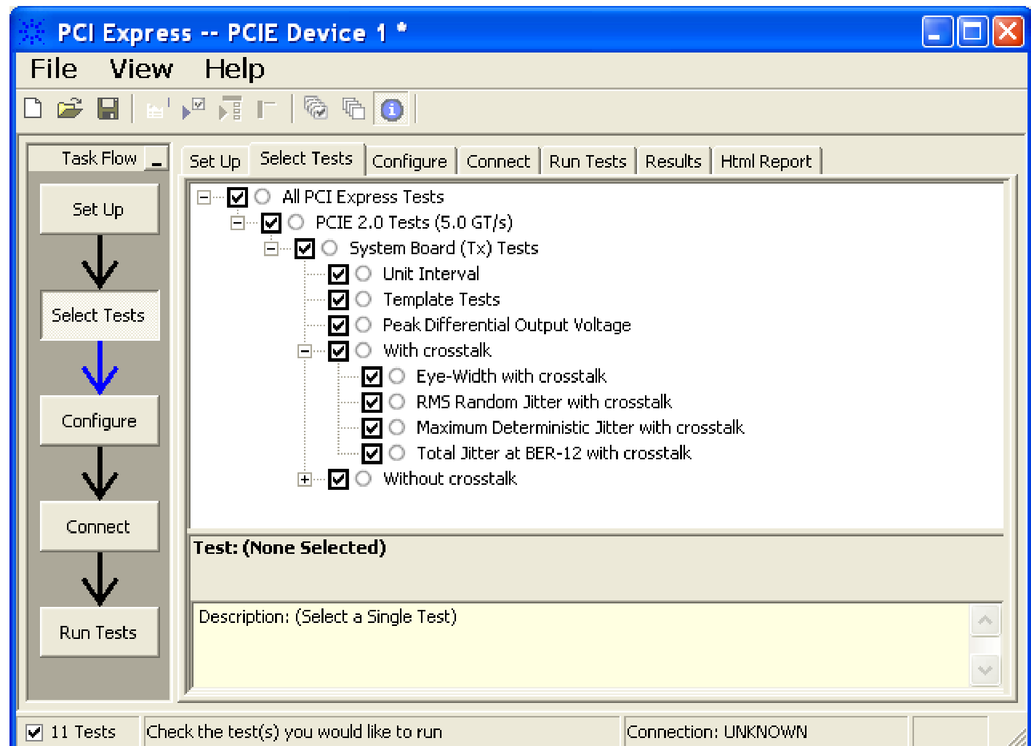


Figure 96 Selecting System Board (Tx) Tests

System Board Tx, Unit Interval

Test ID #:

2400

Test Definition Notes from the Specification

Table 184 Unit Interval from Table 4-9 of the Base Specification: 2.5 and 5.0 GT/s Transmitter Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
UI	Unit Interval	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)	ps	The specified UI is equivalent to a tolerance of ±300 ppm for each Refclk source. Period does not account for SSC caused variations. See below note.

NOTE: SSC permits a +0, -5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33 kHz.

Test Procedure

1 Set the probe point to SYSTEM_TX_2_0.
2 Perform the PreTest function (Utils.xml)

- construct extended FW test steps (e.g. CUST_GetMeasStatsStep, CUST_CancelChecker, etc.).
- check input probe channel setting for “Head Type” configuration.
  - require setting to be N5380A.
  - only applicable for 2-Port testing using 2 differential probes as input.

3 Perform the input signal scaling for display optimization and check the signal characteristics.

- This portion is only done if any of the following item changes:
  - probe point (eg. TX, RX, etc.).
  - the user selectable signal source on the GUI configuration page.
  - the de-embed value on the GUI configuration page.
  - the lane number on the GUI configuration page.
- consist of probe external scaling to cater for signal de-embed option.
- vertical auto-scaling of input signal.
- initialize the FUNC2 as differential source.
- verify if the triggers exist.
- verify that the minimum signal pulse width is within 1 UI range (for NON-RefClk test ONLY).
- verify that the maximum signal pulse width is within 5 UI range (for NON-RefClk test ONLY).

4 Setup labels and grid display settings on the oscilloscope (SetupUI.cmd).

5. Sets the scale and offset of the input channels to their optimum values.
6. Sets the Sample Rate, Enhanced BW, and Memory Depth to the values requested on the configuration page of the GUI.
7. Sets the trigger source and trigger level defined by the user on the configuration page of the GUI.
8. Fit and display all the data sample data on the screen.
9. Use "Unit Interval" measurement on the oscilloscope (EZJit option) and jitter TREND function.
10. Use marker to indicate the upper and lower limit on the FUNC3 (Trend data of UI measurements).
11. Measure UI_max, UI_min and UI_average from FUNC3.
12. Report the measurement results.

Measurement Algorithm

A recovered TX UI is calculated over 3500 consecutive unit intervals of a sample data as the mean unit interval over the clock recovery window.

TX UI(p) = Mean(UI(n))

Where:

n is the index of UI in the clock recovery window.

p indicates the pth 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

Test References

Table 4-9, Section 4.3.3.5, PCI Express Base Specification v2.0.

NOTE The UI measurement is not required at this point. It is provided as an informative test only.

NOTE The TX UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another TX UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The mean TX UI is reported.

System Board Tx, Template Tests

Test ID #:

2410

Test Definition Notes from the Specification

Table 185 System-Board Transmitter Path Compliance Eye Requirements at 5.0 GT/s from Table 4-15 of the Base Specification

Parameter	Min	Max	Unit	Comments
V_{TXS}	300	1200	mV	Notes 1, 2, 4
V_{TXS_d}	300	1200		Notes 1, 2, 4
T_{TXS} (with crosstalk)	95		ps	Notes 1, 3, 4
T_{TXS} (without crosstalk)	108		ps	

NOTES 1: All links are assumed active while generating this eye diagram. The eye diagram requires that CMM pattern *(PCI Express Base Specification, Revision 2.0, Section 4.2.8)* is being transmitted during the test using the de-emphasis level that the system board will use in normal operation.

NOTES 2: Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages.

NOTES 3: T_{TXS} is the minimum eye width. The recommended sample size for this measurement is at least 10^5 UI. This calculated eye width at BER 10^{-12} must not exceed T_{TXS}. If the system board uses non-interleaved routing, then crosstalk will be present in the measurement data. If the system uses interleaved routing, then crosstalk will not be present and an adjusted minimum eye width is used.

NOTES 4: The values in Table 185 are referenced to an ideal 100 Ω differential load at the end of an isolated 3-inch long 85 Ω differential trace behind a standard PCI Express edge finger. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PHY Electrical Test Considerations for PCI Express Architecture* document.

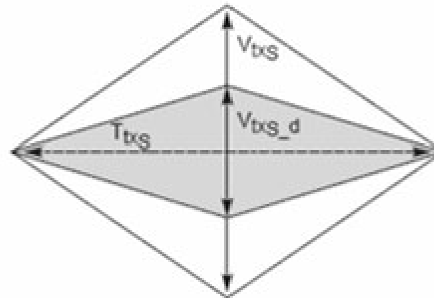


Figure 97 System Board Transmitter Path Composite Compliance Eye Diagram

Test Procedure

1 Set the probe point to SYSTEM_TX_2_0.
2 Perform the PreTest function (Utils.xml)
- construct extended FW test steps (eg. CUST_GetMeasStatsStep, CUST_CancelChecker, etc.).
- check input probe channel setting for “Head Type” configuration.
    - require setting to be N5380A.
    - only applicable for 2-Port testing using 2 differential probes as input.

3 Perform the input signal scaling for display optimization and check the signal characteristics.
- This portion is only done if any of the following item changes:
    - probe point (eg. TX, RX, etc.).
    - the user selectable signal source on the GUI configuration page.
    - the de-embed value on the GUI configuration page.
    - the lane number on the GUI configuration page.
- consist of probe external scaling to cater for signal de-embed option.
- vertical auto-scaling of input signal.
- initialize the FUNC2 as differential source.
- verify if the triggers exist.
- verify that the minimum signal pulse width is within 1 UI range (for NON-RefClk test ONLY).
- verify that the maximum signal pulse width is within 5 UI range (for NON-RefClk test ONLY).

4 Perform the actual compliance testing using the SigTest DLL (CUST_SigTestDLL_SystemBoardTest).
- check if the custom test step has been called in the current trial. This custom test step is designed to execute once per test trial.

- check if the required template file exist. The default template file is “DUAL_PORT_SYS_CON.dat”.
- get the framework configuration variables of interest.
- create plot data directory if it does not exist.
- get the input test waveform data from the oscilloscope (or from Agilent. bin waveform files when running under debug mode only).
- initialize the oscilloscope settings to acquire test waveform data (Scale, Offset, Trigger, Memory depth, etc.).
- acquire the oscilloscope sample waveform data (re-iterate to capture at least 1M UI).
- perform the System compliance test function using the SigTest DLL.
- get the compliance test results from SigTest DLL.
- find and update the worst case test result values.
- calculate the Eye-Width and Differential Peak Output values. These values are used as the final test results in the Eye-Width test and the Differential Peak Output Voltage test.
- Generate the worst filter information (PLL damping factor, PLL frequency and transport delay)
- report the test results to ATE Framework.
- set the flags to indicate that the custom step has been called in the current test trial.

5. Report the measurement results.
6. Display the eye diagrams (transition and non-transition) generated using the SigTest DLL plot data.
7. Check for mask failures in both transition and non-transition eye diagrams. Test will fail if total failures are not equal to zero.

Measurement Algorithm

The system boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-15 of section 4.7.6 of the *PCI Express Card Electromechanical (CEM) Specification, Rev 2.0*, as measured after the connector with an ideal load.

Test References

Table 4-15, Section 4.7.6, PCI Express Base Specification v2.0.

The number of mask violation is 0.

System Board Tx, Peak Differential Output Voltage

Test ID #:

2440

Test Definition Notes from the Specification

Table 186 System Board Transmitter Path Compliance Eye Requirements at 5.0 GT/s from Table 4-15 of the Base Specification

Parameter	Min	Max	Unit	Comments
V_{TXS}	300	1200	mV	Notes 1, 2, 3
V_{TXS_d}	300	1200		Notes 1, 2, 3

NOTES 1: All links are assumed active while generating this eye diagram. The eye diagram requires that CMM pattern *(PCI Express Base Specification, Revision 2.0, Section 4.2.8)* is being transmitted during the test using the de-emphasis level that the system board will use in normal operation.

NOTES 2: Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages.

NOTES 3: The values in Table 186 are referenced to an ideal 100 Ω differential load at the end of an isolated 3-inch long 85 Ω differential trace behind a standard PCI Express edge finger. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PHY Electrical Test Considerations for PCI Express Architecture* document.

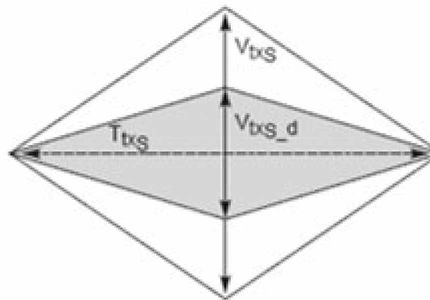


Figure 98 System Board Transmitter Path Composite Compliance Eye Diagram

Test Procedure

1 Set the probe point to SYSTEM_TX_2_0.

2 Perform the PreTest function (Utils.xml)

- construct extended FW test steps (eg. CUST_GetMeasStatsStep, CUST_CancelChecker, etc.).
- check input probe channel setting for “Head Type” configuration.
  - require setting to be N5380A.
  - only applicable for 2-Port testing using 2 differential probes as input.

3 Perform the input signal scaling for display optimization and check the signal characteristics.

- This portion is only done if any of the following item changes:
  - probe point (eg. TX, RX, etc.).
  - the user selectable signal source on the GUI configuration page.
  - the de-embed value on the GUI configuration page.
  - the lane number on the GUI configuration page.
- consist of probe external scaling to cater for signal de-embed option.
- vertical auto-scaling of input signal.
- initialize the FUNC2 as differential source.
- verify if the triggers exist.
- verify that the minimum signal pulse width is within 1 UI range (for NON-RefClk test ONLY).
- verify that the maximum signal pulse width is within 5 UI range (for NON-RefClk test ONLY).

4 Perform the actual compliance testing using the SigTest DLL (CUST_SigTestDLL_SystemBoardTest).

- check if the custom test step has been called in the current trial. This custom test step is designed to execute once per test trial.
- check if the required template file exist. The default template file is “DUAL_PORT_SYS_CON.dat”.
- get the framework configuration variables of interest.
- create plot data directory if it does not exist.
- get the input test waveform data from the oscilloscope (or from Agilent. bin waveform files when running under debug mode only).
- initialize the oscilloscope settings to acquire test waveform data (Scale, Offset, Trigger, Memory depth, etc.).
- acquire the oscilloscope sample waveform data (re-iterate to capture at least 1M UI).

- perform the System Board compliance test function using the SigTest DLL.
- get the compliance test results from SigTest DLL.
- find and update the worst case test result values.
- calculate the Eye-Width and Differential Peak Output values. These values are used as the final test results in the Eye-Width test and the Differential Peak Output Voltage test.
- Generate the worst filter information (PLL damping factor, PLL frequency and transport delay)
- report the test results to ATE Framework.
- set the flags to indicate that the custom step has been called in the current test trial.

5 Report the measurement results.

6 Compare the measured peak voltage (WorstValue) value to the compliance test limits.

Measurement Algorithm

The Differential Peak Voltage measurement returns two times the larger of the Min or Max statistic of the differential voltage waveform.

$V_{TX\text{-}DIFF\text{-}p\text{-}p} = 2 * Max(\ Max(V_{DIFF(i)}), Min(V_{DIFF(i)})\ )$

Where:

i is the index of all waveform values.

V_{DIFF} is the Differential Voltage signal.

Test References

Table 4-15, Section 4.7.6, PCI Express Base Specification v2.0.

The $V_{TX\text{-}DIFF\text{-}p\text{-}p}$ value is within the conformance range limits:

$(300mV <= V_{TX\text{-}DIFF\text{-}p\text{-}p} <= 1.2V)$

System Board Tx, Eye-Width

Test ID #:

2430 (with crosstalk)

2431 (without crosstalk)

Test Definition Notes from the Specification

Table 187 System Board Transmitter Path Compliance Eye Requirements at 5.0 GT/s from Table 4-15 of the Base Specification

Parameter	Min	Max	Unit	Comments
V_{TXS} (with crosstalk)	95		ps	Notes 1, 2, 3
V_{TXS} (without crosstalk)	108		ps	

NOTES 1: All links are assumed active while generating this eye diagram. The eye diagram requires that CMM pattern *(PCI Express Base Specification, Revision 2.0, Section 4.2.8)* is being transmitted during the test using the de-emphasis level that the system board will use in normal operation.

NOTES 2: T_{TXS} is the minimum eye width. The recommended sample size for this measurement is at least 10^5 UI. This calculated eye width at BER 10^{-12} must not exceed T_{TXS}. If the system board uses non-interleaved routing, then crosstalk will be present in the measurement data. If the system uses interleaved routing, then crosstalk will not be present and an adjusted minimum eye width is used.

NOTES 3: The values in Table 187 are referenced to an ideal 100 Ω differential load at the end of an isolated 3-inch long 85 Ω differential trace behind a standard PCI Express edge finger. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PHY Electrical Test Considerations for PCI Express Architecture* document.

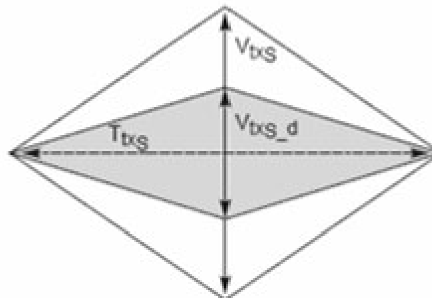


Figure 99 System Board Transmitter Path Compliance Eye Diagram

Test Procedure

1 Set the probe point to SYSTEM_TX_2_0.
2 Perform the PreTest function (Utils.xml)

- construct extended FW test steps (eg. CUST_GetMeasStatsStep, CUST_CancelChecker, etc.).
- check input probe channel setting for "Head Type" configuration.
  - require setting to be N5380A.
  - only applicable for 2-Port testing using 2 differential probes as input.

3 Perform the input signal scaling for display optimization and check the signal characteristics.

- This portion is only done if any of the following item changes:
  - probe point (eg. TX, RX, etc.).
  - the user selectable signal source on the GUI configuration page.
  - the de-embed value on the GUI configuration page.
  - the lane number on the GUI configuration page.
- consist of probe external scaling to cater for signal de-embed option.
- vertical auto-scaling of input signal.
- initialize the FUNC2 as differential source.
- verify if the triggers exist.
- verify that the minimum signal pulse width is within 1 UI range (for NON-RefClk test ONLY).
- verify that the maximum signal pulse width is within 5 UI range (for NON-RefClk test ONLY).

4 Perform the actual compliance testing using the SigTest DLL (CUST_SigTestDLL_SystemBoardTest).

- check if the custom test step has been called in the current trial. This custom test step is designed to execute once per test trial.
- check if the required template file exist. The default template file is "DUAL_PORT_SYS_CON.dat".
- get the framework configuration variables of interest.
- create plot data directory if it does not exist.
- get the input test waveform data from the oscilloscope (or from Agilent. bin waveform files when running under debug mode only).
- initialize the oscilloscope settings to acquire test waveform data (Scale, Offset, Trigger, Memory depth, etc.).
- acquire the oscilloscope sample waveform data (re-iterate to capture at least 1M UI).
- perform the system board compliance test function using the SigTest DLL.
- get the compliance test results from SigTest DLL.
- find and update the worst case test result values.

- calculate the Eye-Width and Differential Peak Output values. These values are used as the final test results in the Eye-Width test and the Differential Peak Output Voltage test.
- Generate worst filter information (PLL damping factor, PLL frequency and transport delay).
- report the test results to ATE Framework.
- set the flags to indicate that the custom step has been called in the current test trial.

5 Report the measurement results.

6 Compare the measured eye-width value to the compliance test limits.

Measurement Algorithm

This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [total jitter at BER-12]. This parameter is measured with the equivalent of a zero jitter reference clock.

There are 4 different test IDs for the system Board Eye Width Tests as follow. The test procedure is the same for these tests with the exception of the template files and compliance test limits (with and without crosstalk).

a System Board Tx, Eye-Width with crosstalk (PCIE 2.0): ID# 2430

b system Board Tx, Eye-Width without crosstalk (PCIE 2.0): ID# 2431

Test References

Table 4-15, Section 4.7.6, PCI Express Base Specification v2.0.

The measured eye width value shall be greater than 95 ps (without crosstalk) or 108 ps (with crosstalk).

System Board Tx, RMS Random Jitter

Test ID #:

2482 (with crosstalk)

2483 (without crosstalk)

Test Definition Notes from the Specification

Table 188 System Board Jitter Requirement for 5 GT/s Signaling: from Table 4-16 of the Base Specification

Parameter	Max Dj (ps)	Tj at BER 10^{-12} (ps)
With crosstalk	57	105
Without crosstalk	44	92

Test Procedure

1 Set the probe point to SYSTEM_TX_2_0.

2 Perform the PreTest function (Utils.xml)

- construct extended FW test steps (eg. CUST_GetMeasStatsStep, CUST_CancelChecker, etc.).
- check input probe channel setting for “Head Type” configuration.
    - require setting to be N5380A.
    - only applicable for 2-Port testing using 2 differential probes as input.

3 Perform the input signal scaling for display optimization and check the signal characteristics.

- This portion is only done if any of the following item changes:
    - probe point (eg. TX, RX, etc.).
    - the user selectable signal source on the GUI configuration page.
    - the de-embed value on the GUI configuration page.
    - the lane number on the GUI configuration page.
- consist of probe external scaling to cater for signal de-embed option.
- vertical auto-scaling of input signal.
- initialize the FUNC2 as differential source.
- verify if the triggers exist.
- verify that the minimum signal pulse width is within 1 UI range (for NON-RefClk test ONLY).
- verify that the maximum signal pulse width is within 5 UI range (for NON-RefClk test ONLY).

4 Perform the actual compliance testing using the SigTest DLL (CUST_SigTestDLL_SystemBoardTest).

- check if the custom test step has been called in the current trial. This custom test step is designed to execute once per test trial.
- check if the required template file exist. The default template file is “DUAL_PORT_SYS_CON.dat”.
- get the framework configuration variables of interest.
- create plot data directory if it does not exist.
- get the input test waveform data from the oscilloscope (or from Agilent. bin waveform files when running under debug mode only).
- initialize the oscilloscope settings to acquire test waveform data (Scale, Offset, Trigger, Memory depth, etc.).
- acquire the oscilloscope sample waveform data (re-iterate to capture at least 1M UI).

- perform the System Board compliance test function using the SigTest DLL.
- get the compliance test results from SigTest DLL.
- find and update the worst case test result values.
- calculate the Eye-Width and Differential Peak Output values. These values are used as the final test results in the Eye-Width test and the Differential Peak Output Voltage test.
- generate worst filter information (PLL damping factor, PLL frequency and transport delay)
- report the test results to ATE Framework.
- set the flags to indicate that the custom step has been called in the current test trial.

5. Report the measurement results.
6. Compare the measured Random Jitter value to the compliance test limits.

Measurement Algorithm

This is a timing measurement in PCI Express Gen2 that requires separation of the high frequency jitter on the transmitter signal.

The transmitter is tested with a low jitter reference clock (clean clock). However, the reference clock may still have some low frequency wander. Besides that, the transmitter itself may have low frequency wander from VDD (supply voltage), temperature and other affects. In order to avoid this increasing observed transmitter jitter, jitter on the recovered clock is separated into different bands and measured.

1. High frequency jitter (above 1.5 MHz) that is not tracked by the receiver and therefore reduces the transmitter eye width.
2. Low frequency jitter (10kHz - 1.5MHz) that is mostly tracked by the receiver and used as part of the receiver testing.
3. Jitter below 10 kHz that is considered wander or drift and are tracked by the receiver.

There are 2 different test IDs for the System Board Maximum Deterministic Jitter Tests as follow. The test procedure is the same for these tests with the exception of the template files and compliance test limits (with and without crosstalk).

a. System Board Tx, RMS Random Jitter with crosstalk (PCIE 2.0): ID# 2482
b. System Board Tx, RMS Random Jitter without crosstalk (PCIE 2.0): ID# 2483

Test References

Table 4-16, Section 4.7.6, PCI Express Base Specification v2.0.

The measured Deterministic Jitter value for the test signal shall be within the conformance limit value of (TJ_{BER-12} - DJ_{Max}).

System Board Tx, Maximum Deterministic Jitter

Test ID #:

2492 (with crosstalk)

2493 (without crosstalk)

Test Definition Notes from the Specification

Table 189 System Board Jitter Requirement for 5 GT/s Signaling: from Table 4-16 of the Base Specification

Parameter	Max Dj (ps)
With crosstalk	57
Without crosstalk	44

Test Procedure

1 Set the probe point to SYSTEM_TX_2_0.
2 Perform the PreTest function (Utils.xml)

- construct extended FW test steps (eg. CUST_GetMeasStatsStep, CUST_CancelChecker, etc.).
- check input probe channel setting for “Head Type” configuration.
  - require setting to be N5380A.
  - only applicable for 2-Port testing using 2 differential probes as input.

3 Perform the input signal scaling for display optimization and check the signal characteristics.

- This portion is only done if any of the following item changes:
  - probe point (eg. TX, RX, etc.).
  - the user selectable signal source on the GUI configuration page.
  - the de-embed value on the GUI configuration page.
  - the lane number on the GUI configuration page.
- consist of probe external scaling to cater for signal de-embed option.
- vertical auto-scaling of input signal.

- initialize the FUNC2 as differential source.
- verify if the triggers exist.
- verify that the minimum signal pulse width is within 1 UI range (for NON-RefClk test ONLY).
- verify that the maximum signal pulse width is within 5 UI range (for NON-RefClk test ONLY).

4 Perform the actual compliance testing using the SigTest DLL (CUST_SigTestDLL_SystemBoardTest).

- check if the custom test step has been called in the current trial. This custom test step is designed to execute once per test trial.
- check if the required template file exist. The default template file is “DUAL_PORT_SYS_CON.dat”.
- get the framework configuration variables of interest.
- create plot data directory if it does not exist.
- get the input test waveform data from the oscilloscope (or from Agilent.bin waveform files when running under debug mode only).
- initialize the oscilloscope settings to acquire test waveform data (Scale, Offset, Trigger, Memory depth, etc.).
- acquire the oscilloscope sample waveform data (re-iterate to capture at least 1M UI).
- perform the system board compliance test function using the SigTest DLL.
- get the compliance test results from SigTest DLL.
- find and update the worst case test result values.
- calculate the Eye-Width and Differential Peak Output values. These values are used as the final test results in the Eye-Width test and the Differential Peak Output Voltage test.
- generate worst filter information (PLL damping factor, PLL frequency and transport delay).
- report the test results to ATE Framework.
- set the flags to indicate that the custom step has been called in the current test trial.

5 Report the measurement results.

6 Compare the measured Deterministic Jitter value to the compliance test limits.

Measurement Algorithm

This is a timing measurement in PCI Express Gen2 that requires separation of the high frequency jitter on the transmitter signal.

The transmitter is tested with a low jitter reference clock (clean clock). However, the reference clock may still have some low frequency wander. Besides that, the transmitter itself may have low frequency wander from VDD (supply voltage), temperature and other affects. In order to avoid this increasing observed transmitter jitter, jitter on the recovered clock is separated into different bands and measured.

1 High frequency jitter (above 1.5 MHz) that is not tracked by the receiver and therefore reduces the transmitter eye width.
2 Low frequency jitter (10kHz - 1.5MHz) that is mostly tracked by the receiver and used as part of the receiver testing.
3 Jitter below 10 kHz that is considered wander or drift and are tracked by the receiver.

There are 4 different test IDs for the System Board Maximum Jitter Tests as follow. The test procedure is the same for these tests with the exception of the template files and compliance test limits (both with and without crosstalk).

- a System Board Tx, Maximum Deterministic Jitter with crosstalk (PCIE 2.0): ID# 2492
- b System Board Tx, Maximum Deterministic Jitter without crosstalk (PCIE 2.0): ID# 2493

Test References

Table 4-16, Section 4.7.6, PCI Express Base Specification v2.0.

System Board Tx, Total Jitter at BER-12

Test ID #:

2496 (with crosstalk)

2497 (without crosstalk)

Test Definition Notes from the Specification

Table 190 System Board Jitter Requirement for 5 GT/s Signaling: from Table 4-16 of the Base Specification

Parameter	Max Dj (ps)
With crosstalk	105
Without crosstalk	92

Test Procedure

1 Set the probe point to SYSTEM_TX_2_0.
2 Perform the PreTest function (Utils.xml)

- construct extended FW test steps (eg. CUST_GetMeasStatsStep, CUST_CancelChecker, etc.).
- check input probe channel setting for “Head Type” configuration.
  - require setting to be N5380A.
  - only applicable for 2-Port testing using 2 differential probes as input.

3 Perform the input signal scaling for display optimization and check the signal characteristics.

- This portion is only done if any of the following item changes:
  - probe point (eg. TX, RX, etc.).
  - the user selectable signal source on the GUI configuration page.
  - the de-embed value on the GUI configuration page.
  - the lane number on the GUI configuration page.
- consist of probe external scaling to cater for signal de-embed option.
- vertical auto-scaling of input signal.
- initialize the FUNC2 as differential source.
- verify if the triggers exist.
- verify that the minimum signal pulse width is within 1 UI range (for NON-RefClk test ONLY).
- verify that the maximum signal pulse width is within 5 UI range (for NON-RefClk test ONLY).

4 Perform the actual compliance testing using the SigTest DLL (CUST_SigTestDLL_SystemBoardTest).

- check if the custom test step has been called in the current trial. This custom test step is designed to execute once per test trial.
- check if the required template file exist. The default template file is “DUAL_PORT_SYS_CON.dat”.
- get the framework configuration variables of interest.
- create plot data directory if it does not exist.
- get the input test waveform data from the oscilloscope (or from Agilent. bin waveform files when running under debug mode only).
- initialize the oscilloscope settings to acquire test waveform data (Scale, Offset, Trigger, Memory depth, etc.).
- acquire the oscilloscope sample waveform data (re-iterate to capture at least 1M UI).

- perform the System Board compliance test function using the SigTest DLL.
- get the compliance test results from SigTest DLL.
- find and update the worst case test result values.
- calculate the Eye-Width and Differential Peak Output values. These values are used as the final test results in the Eye-Width test and the Differential Peak Output Voltage test.
- generate the worst filter information (PLL damping factor, PLL frequency and transport delay).
- report the test results to ATE Framework.
- set the flags to indicate that the custom step has been called in the current test trial.

5 Report the measurement results.

6 Compare the measured Total Jitter at BER-12 value to the compliance test limits.

Measurement Algorithm

This is a timing measurement in PCI Express Gen2 that requires separation of the high frequency jitter on the transmitter signal.

The transmitter is tested with a low jitter reference clock (clean clock). However, the reference clock may still have some low frequency wander. Besides that, the transmitter itself may have low frequency wander from VDD (supply voltage), temperature and other affects. In order to avoid this increasing observed transmitter jitter, jitter on the recovered clock is separated into different bands and measured.

1. High frequency jitter (above 1.5 MHz) that is not tracked by the receiver and therefore reduces the transmitter eye width.
2. Low frequency jitter (10kHz - 1.5MHz) that is mostly tracked by the receiver and used as part of the receiver testing.
3. Jitter below 10 kHz that is considered wander or drift and are tracked by the receiver.

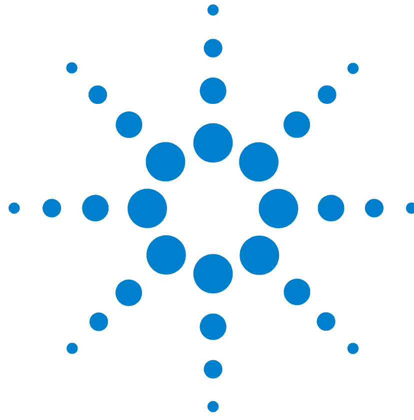
There are 2 different test IDs for the System Board Total Jitter at BER-12 Tests as follow. The test procedure is the same for these tests with the exception of the template files and compliance test limits (with and without crosstalk).

a. System Board Tx, Total Jitter at BER-12 with crosstalk (PCIE 2.0): ID# 2496

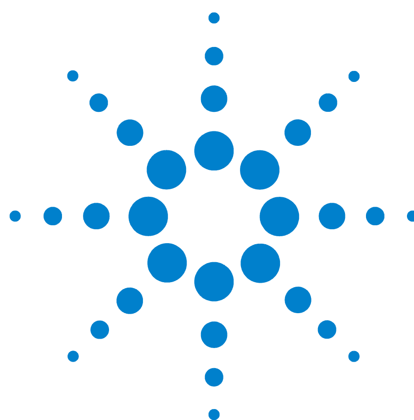
b. System Board Tx, Total Jitter at BER-12 without crosstalk (PCIE 2.0): ID# 2497

Test References

Table 4-16, Section 4.7.6, PCI Express Base Specification v2.0.



Part VI
ExpressCard 1.0



20
ExpressCard Tests

ExpressCard Module Tx Tests 351
ExpressCard Host Tx Tests 359

This section provides the Methods of Implementation (MOIs) for ExpressCard tests using an Agilent 54855A, 80000B, or 90000A series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

ExpressCard Module Tx Tests

Probing the Link for ExpressCard Module Compliance

Consult the *PHY Electrical Test Specification for PCI Express Architecture* and the *ExpressCard Standard, Release 1.0* for instructions to connect for testing the ExpressCard module transmitter path.

Ensure the proper polarity.

Running ExpressCard Module Tx Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 22. At the Set Up page, select "Express Card 1.0". Then, when selecting tests, navigate to the "ExpressCard Module Tx Tests" group.

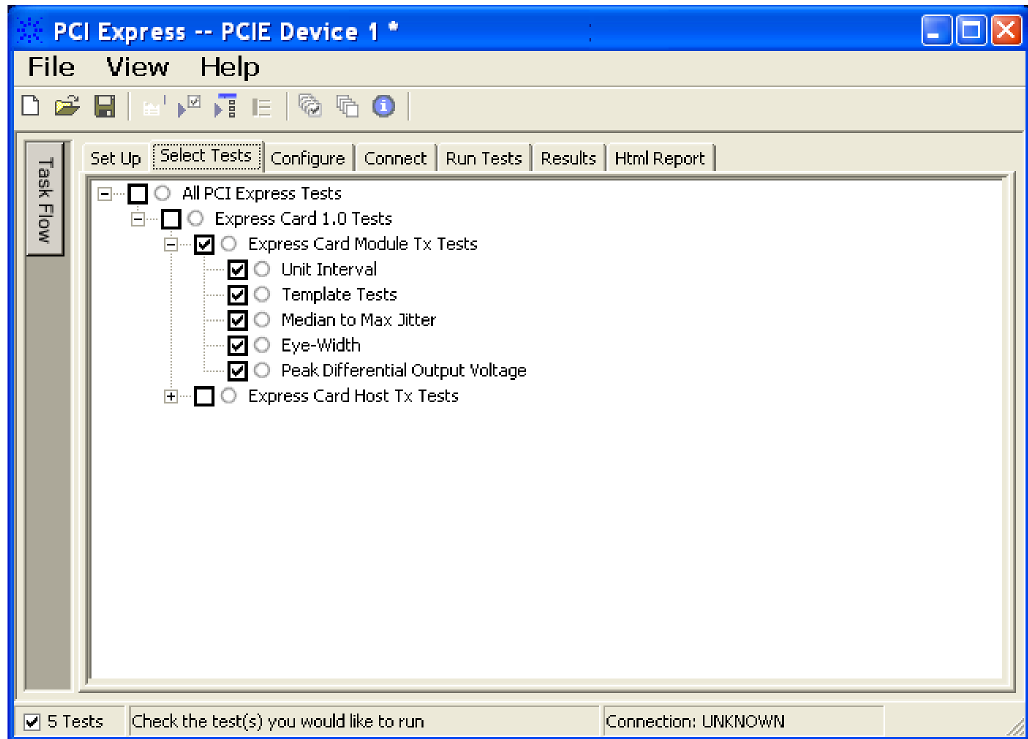


Figure 100 Selecting ExpressCard Module Tx Tests

ExpressCard Module Tx, Unit Interval

Table 191 UI from Table 4-5 of the Base Specification

Symbol	Parameter	Min	Nom	Max
UI	Unit Interval	399.88 ps	400ps	400.12 ps

Test Definition Notes from the Specification

- UI (Unit Interval) is specified to be +/-300 ppm.
- UI does not account for SSC dictated variations.
- UI is defined in Table 4-5 (Base Specification).
- UI Characteristics are Maximum UI =400.12 ps and Minimum UI = 399.88ps.

Test Procedure

Follow the procedure in “ExpressCard Module Tx Tests" on page 351, and select “ExpressCard Module Tx, Unit Interval”.

PASS Condition

399.88ps < UI < 400.12ps

Measurement Algorithm

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window.

TX UI(p) = Mean(UI(n))

Where:

n is the index of UI in the clock recovery window.

p indicates the pth 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI, as described below.

NOTE The UI measurement is not required at this point. It is provided as an informative test only.

NOTE The TX UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another TX UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case TX UI is reported.

Test References

Table 192 ExpressCard Module Tx, Unit Interval Test References

Test Name	Reference	PCI-SIG Assertions
ExpressCard Module Tx, Unit Interval	This test is not required. It is informative only.	

ExpressCard Module Tx, Template Tests

See Section 4.2.1.3.1 of the ExpressCard Standard for additional notes and test definitions.

Test Definition Notes from the Specification

Table 193 Table 4-3 of the ExpressCard Standard

Parameter	Value	Notes
Vtx_A	>= 538 mV	All Links are assumed active while generating this eye diagram. Transition and nontransition bits must be distinguished in order to measure compliance against the deemphasized voltage level (Ttx_A_d).
Vtx_A_d	>= 368 mV	
Ttx_A	>= 237 ps	

- Note: The values in Table 193 are referenced to an ideal 100 ohm differential load at the end of the interconnect path at the isolated edge-finger boundary of an add-in card when mated with a connector. The eye diagram is defined and centered with respect to the jitter median. The jitter median should be calculated across any 250 consecutive UIs. The maximum jitter outlier should be no greater than 81.5 ps away from the jitter median.

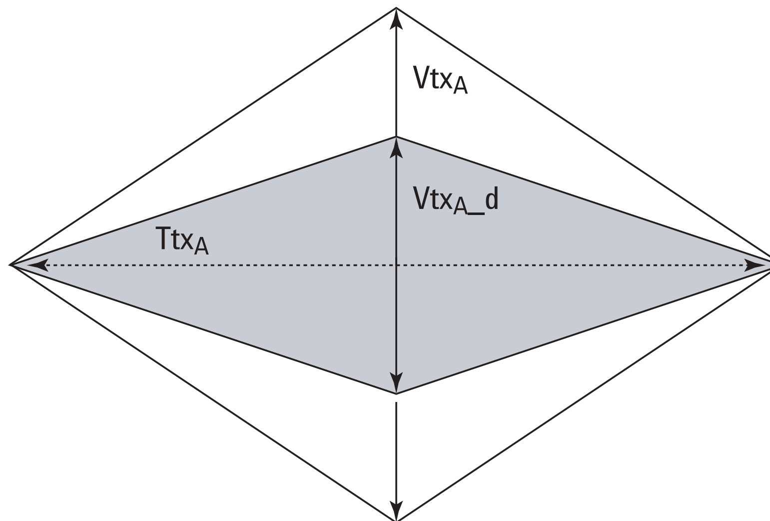


Figure 101 ExpressCard Module Tx Compliance Eye Diagram

Test References

Table 194 ExpressCard Module Tx, Template Tests Test References

Test Name	Reference	PCI-SIG Assertions
ExpressCard Module Tx, Template Tests	ExpressCard Standard, Release 1.0, Table 4-3	

ExpressCard Module Tx, Median to Max Jitter

Table 195 $Ttx_{A\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ for ExpressCard

Symbol	Parameter	Min	Nom	Max
$Ttx_{A\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	Maximum time between the jitter median and maximum deviation from the median.			81.5 ps

Test Definition Notes from the Specification

- Jitter is defined as the measurement variation of the crossing points ($V_{TX\text{-}DIFFp\text{-}p}$ = 0 V) in relation to the recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used to calculate the TX UI.
- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured over any 250 consecutive TX UIs. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).
- A Ttx_A >= 237 ps provides for a total sum of deterministic and random jitter budget of $Ttx_{A\text{-}MAX\text{-}JITTER}$ = 163 ps for the Transmitter collected over any 250 consecutive TX UIs. The $Ttx_{A\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs.

  It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
- $Ttx_{A\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ (Maximum time between the jitter median and maximum deviation from the median) is derived from Table 4-3 in the ExpressCard Standard.

Limits

Maximum = 81.5 ps

Pass Condition

81.5 ps > $Ttx_{A\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$.

Test Procedure

Follow the procedure in "ExpressCard Module Tx Tests" on page 351, and select "ExpressCard Module Tx, Median to Max Jitter".

Measurement Algorithm

This measurement is made over 250 consecutive bits defined in Section 3.4 (Base Specification).

The measured time difference between a data edge and a recovered clock edge.

$$tie(n) = t_{R-DAT}(n) - t_{DAT}(n)$$

Where:

t_{DAT} is the original data edge.

t_{R-DAT} is the recovered data edge (the ideal time of the data edge as defined by the recovered clock around t_{DAT}).

n is the index of all edges in the waveform.

Test References

Table 196 ExpressCard Module Tx, Median to Max Jitter Test References

Test Name	Reference	PCI-SIG Assertions
ExpressCard Module Tx, Median to Max Jitter	ExpressCard Standard, Release 1.0, Table 4-3	

ExpressCard Module Tx, Eye-Width

Table 197 Ttx_A for ExpressCard

Symbol	Parameter	Min	Nom	Max
Ttx_A	Minimum TX Eye Width	237 ps		

Test Definition Notes from the Specification

- The maximum Transmitter jitter can be derived as $Ttx_{A-MAX-JITTER} = 400\ ps - Ttx_A = 163\ ps$.

- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured over any 250 consecutive TX UIs. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).
- A Ttx_A = 237 ps provides for a total sum of deterministic and random jitter budget of $Ttx_{A-MAX-JITTER}$ = 163 ps for the Transmitter collected over any 250 consecutive TX UIs. The $Ttx_{A-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs.

NOTE The median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

- Ttx_A (Minimum TX Eye Width) is defined in Table 4-3 of the ExpressCard Standard.

Limits

Minimum = 237 ps

Pass Condition

237 ps <= Ttx_A

Test Procedure

Follow the procedure in “ExpressCard Module Tx Tests" on page 351, and select “ExpressCard Module Tx, Eye-Width”.

Measurement Algorithm

This measurement is made over 250 consecutive bits defined in Section 3.4 (Base Specification).

The measured minimum horizontal eye opening at the zero reference level as shown in the eye diagram.

$$T_{EYE-WIDTH} = UI_{AVG} - TIE_{Pk-Pk}$$

Where:

UI_{AVG} is the average UI.

TIE_{Pk-Pk} is the Peak-Peak TIE.

Test References

Table 198 ExpressCard Module Tx, Eye-Width Test References

Test Name	Reference	PCI-SIG Assertions
ExpressCard Module Tx, Eye-Width	ExpressCard Standard, Release 1.0, Table 4-3	

ExpressCard Module Tx, Peak Differential Output Voltage

Table 199 $V_{TX\text{-}DIFFp\text{-}p}$ for ExpressCard

Symbol	Parameter	Min	Nom	Max
$V_{TX\text{-}DIFFp\text{-}p}$	Differential Pk-Pk Output Voltage	0.368 V		1.2 V

Test Definition Notes from the Specification

- $V_{TX\text{-}DIFFp\text{-}p} = 2*|V_{TX\text{-}D+} - V_{TX\text{-}D-}|$
- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured over any 250 consecutive TX UIs. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).

Test Procedure

Follow the procedure in “ExpressCard Module Tx Tests" on page 351, and select “ExpressCard Module Tx, Peak Differential Output Voltage”.

PASS Condition

$0.368\ V <= V_{TX\text{-}DIFF\text{-}p\text{-}p} <= 1.2V$

Measurement Algorithm

The Differential Peak Voltage measurement returns two times the larger of the Min or Max statistic if the differential voltage waveform.

$$V_{TX\text{-}DIFF\text{-}p\text{-}p} = 2*Max(\ Max(V_{DIFF(i)}),\ Min(V_{DIFF(i)}))$$

Where:

i is the index of all waveform values.

V_{DIFF} is the Differential Voltage signal.

Test References

Table 200 ExpressCard Module Tx, Peak Differential Output Voltage Test References

Test Name	Reference	PCI-SIG Assertions
ExpressCard Module Tx, Peak Differential Output Voltage	ExpressCard Standard, Release 1.0, Table 4-3	

ExpressCard Host Tx Tests

Probing the Link for ExpressCard Host Compliance

Consult the *PHY Electrical Test Specification for PCI Express Architecture* and the *ExpressCard Standard, Release 1.0* for instructions to connect for testing the ExpressCard host transmitter path.

Ensure the proper polarity.

Running ExpressCard Host Tx Tests

Start the automated testing application as described in “Starting the PCI Express Automated Test Application" on page 22. At the Set Up page, select “Express Card 1.0”. Then, when selecting tests, navigate to the “ExpressCard Host Tx Tests” group.

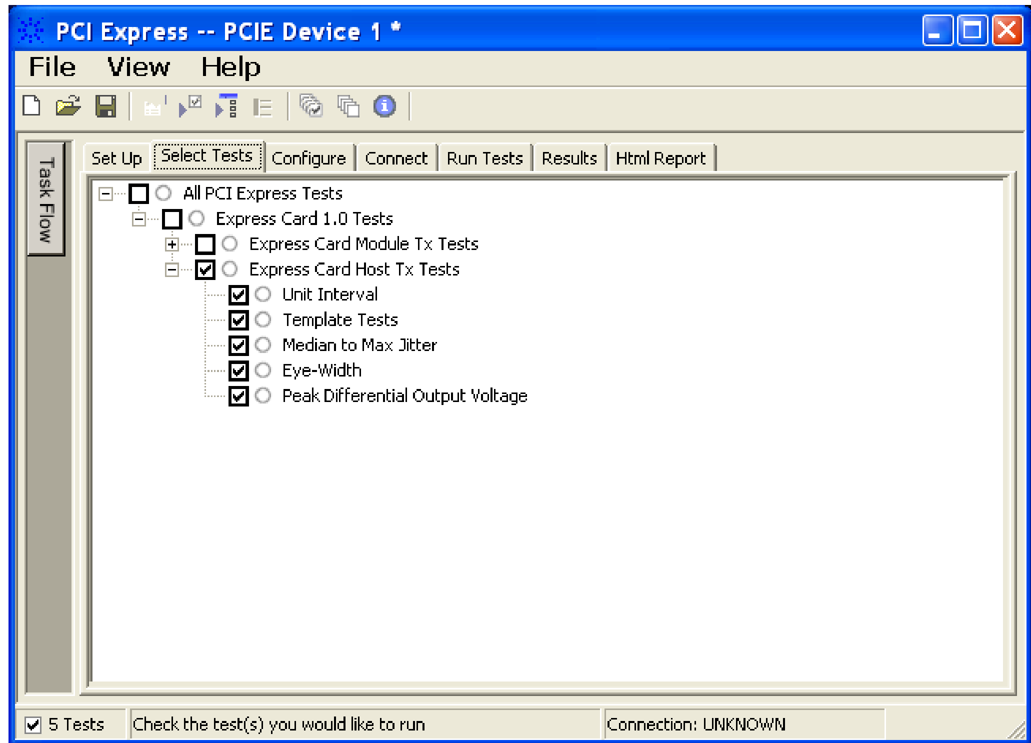


Figure 102 Selecting ExpressCard Host Tx Tests

ExpressCard Host Tx, Unit Interval

Table 201 UI from Table 4-5 of the Base Specification

Symbol	Parameter	Min	Nom	Max
UI	Unit Interval	399.88 ps	400ps	400.12 ps

Test Definition Notes from the Specification

- UI (Unit Interval) is specified to be +/-300 ppm.
- UI does not account for SSC dictated variations.
- UI is defined in Table 4-5 (Base Specification).
- UI Characteristics are Maximum UI =400.12 ps and Minimum UI = 399.88ps.

Test Procedure

Follow the procedure in “Test References" on page 359, and select “ExpressCard Host Tx, Unit Interval”.

PASS Condition

399.88ps < UI < 400.12ps

Measurement Algorithm

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window.

TX UI(p) = Mean(UI(n))

Where:

n is the index of UI in the clock recovery window.

p indicates the pth 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI, as described below.

NOTE The UI measurement is not required at this point. It is provided as an informative test only.

NOTE The TX UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another TX UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case TX UI is reported.

Test References

Table 202 ExpressCard Host Tx, Unit Interval Test References

Test Name	Reference	PCI-SIG Assertions
ExpressCard Host Tx, Unit Interval	This test is not required. It is informative only.	

ExpressCard Host Tx, Template Tests

See Section 4.2.1.3.3 of the ExpressCard Standard for additional notes and test definitions.

Test Definition Notes from the Specification

Table 203 Table 4-5 of the ExpressCard Standard

Parameter	Value	Notes
Vtx_S	>= 262 mV	All Links are assumed active while generating this eye diagram. Transition and nontransition bits must be distinguished in order to measure compliance against the deemphasized voltage level (Ttx_S_d).
Vtx_S_d	>= 247 mV	
Ttx_S	>= 183 ps	

- Note: The values in Table 203 are referenced to an ideal 100 ohm differential load at the end of the interconnect path at the isolated edge-finger boundary of an add-in card when mated with a connector. The eye diagram is defined and centered with respect to the jitter median. The jitter median should be calculated across any 250 consecutive UIs. The maximum jitter outlier should be no greater than 108.5 ps away from the jitter median.

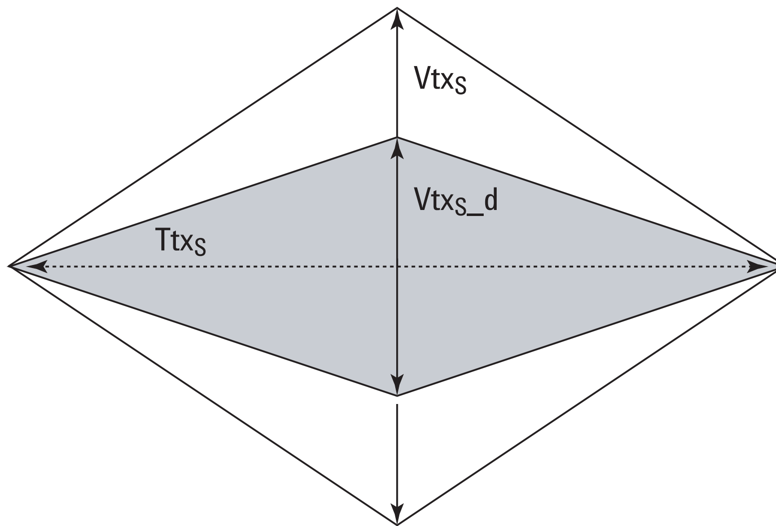


Figure 103 ExpressCard Host Tx Compliance Eye Diagram

Test References

Table 204 ExpressCard Host Tx, Template Tests Test References

Test Name	Reference	PCI-SIG Assertions
ExpressCard Host Tx, Template Tests	ExpressCard Standard, Release 1.0, Table 4-5	

ExpressCard Host Tx, Median to Max Jitter

Table 205 $Ttx_{S\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ for ExpressCard

Symbol	Parameter	Min	Nom	Max
$Ttx_{S\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	Maximum time between the jitter median and maximum deviation from the median.			108.5 ps

Test Definition Notes from the Specification

- Jitter is defined as the measurement variation of the crossing points ($V_{TX\text{-}DIFFp\text{-}p}$ = 0 V) in relation to the recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used to calculate the TX UI.
- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured over any 250 consecutive TX UIs. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).
- A Ttx_S >= 183 ps provides for a total sum of deterministic and random jitter budget of $Ttx_{S\text{-}MAX\text{-}JITTER}$ = 217 ps for the Transmitter collected over any 250 consecutive TX UIs. The $Ttx_{S\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs.

  It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
- $Ttx_{S\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ (Maximum time between the jitter median and maximum deviation from the median) is derived from Table 4-5 in the ExpressCard Standard.

Limits

Maximum = 108.5 ps

Pass Condition

108.5 ps > $Ttx_{S\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$.

Test Procedure

Follow the procedure in “Test References" on page 359, and select “ExpressCard Host Tx, Median to Max Jitter”.

Measurement Algorithm

This measurement is made over 250 consecutive bits defined in Section 3.4 (Base Specification).

The measured time difference between a data edge and a recovered clock edge.

$$tie(n) = t_{R-DAT}(n) - t_{DAT}(n)$$

Where:

t_{DAT} is the original data edge.

t_{R-DAT} is the recovered data edge (the ideal time of the data edge as defined by the recovered clock around t_{DAT}).

n is the index of all edges in the waveform.

Test References

Table 206 ExpressCard Host Tx, Median to Max Jitter Test References

Test Name	Reference	PCI-SIG Assertions
ExpressCard Host Tx, Median to Max Jitter	ExpressCard Standard, Release 1.0, Table 4-5	

ExpressCard Host Tx, Eye-Width

Table 207 Ttx_S for ExpressCard

Symbol	Parameter	Min	Nom	Max
Ttx_S	Minimum TX Eye Width	183 ps		

Test Definition Notes from the Specification

- The maximum Transmitter jitter can be derived as $Ttx_{S-MAX-JITTER} = 400\text{ ps} - Ttx_S = 217\text{ ps}$.

- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured over any 250 consecutive TX UIs. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).
- A Ttx_S = 183 ps provides for a total sum of deterministic and random jitter budget of $Ttx_{S-MAX-JITTER}$ = 217 ps for the Transmitter collected over any 250 consecutive TX UIs. The $Ttx_{S-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs.

NOTE

The median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

- Ttx_S (Minimum TX Eye Width) is defined in Table 4-5 of the ExpressCard Standard.

Limits

Minimum = 183 ps

Pass Condition

183 ps <= Ttx_S.

Test Procedure

Follow the procedure in “Test References" on page 359, and select “ExpressCard Host Tx, Eye-Width”.

Measurement Algorithm

This measurement is made over 250 consecutive bits defined in Section 3.4 (Base Specification).

The measured minimum horizontal eye opening at the zero reference level as shown in the eye diagram.

$$T_{EYE-WIDTH} = UI_{AVG} - TIE_{Pk-Pk}$$

Where:

UI_{AVG} is the average UI.

TIE_{Pk-Pk} is the Peak-Peak TIE.

Test References

Table 208 ExpressCard Host Tx, Eye-Width Test References

Test Name	Reference	PCI-SIG Assertions
ExpressCard Host Tx, Eye-Width	ExpressCard Standard, Release 1.0, Table 4-5	

ExpressCard Host Tx, Peak Differential Output Voltage

Table 209 $V_{TX\text{-}DIFFp\text{-}p}$ for ExpressCard

Symbol	Parameter	Min	Nom	Max
$V_{TX\text{-}DIFFp\text{-}p}$	Differential Pk-Pk Output Voltage	0.247 V		1.2 V

Test Definition Notes from the Specification

- $V_{TX\text{-}DIFFp\text{-}p} = 2*|V_{TX\text{-}D+} - V_{TX\text{-}D-}|$
- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured over any 250 consecutive TX UIs. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).

Test Procedure

Follow the procedure in “Test References" on page 359, and select “ExpressCard Host Tx, Peak Differential Output Voltage”.

PASS Condition

$0.247\ V <= V_{TX\text{-}DIFF\text{-}p\text{-}p} <= 1.2V$

Measurement Algorithm

The Differential Peak Voltage measurement returns two times the larger of the Min or Max statistic if the differential voltage waveform.

$$V_{TX\text{-}DIFF\text{-}p\text{-}p} = 2*Max(Max(V_{DIFF(i)}), Min(V_{DIFF(i)}))$$

Where:

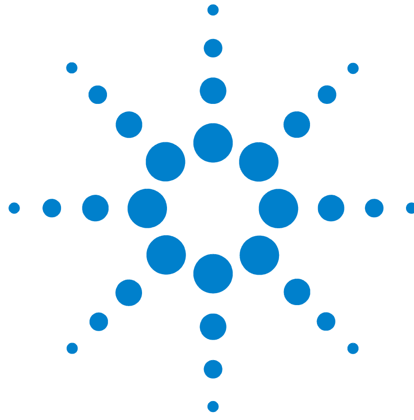
i is the index of all waveform values.

V_{DIFF} is the Differential Voltage signal.

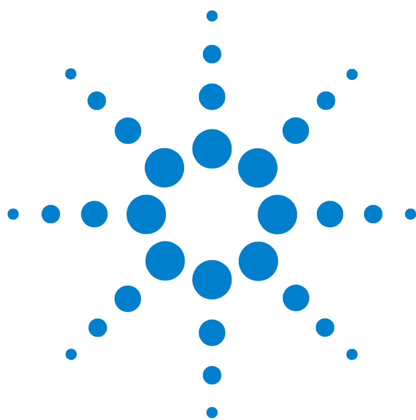
Test References

Table 210 ExpressCard Host Tx, Peak Differential Output Voltage Test References

Test Name	Reference	PCI-SIG Assertions
ExpressCard Host Tx, Peak Differential Output Voltage	ExpressCard Standard, Release 1.0, Table 4-5	



Part VII
Appendices



A
Calibrating the Digital Storage Oscilloscope

Required Equipment for Calibration 370
Internal Calibration 371
Cable and Probe Calibration 377
Channel-to-Channel De-skew 386

This appendix describes the Agilent digital storage oscilloscope calibration procedures.

Required Equipment for Calibration

To calibrate the oscilloscope in preparation for running the PCI Express automated tests, you need the following equipment:

- Keyboard, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Precision 3.5 mm BNC to SMA male adapter, Agilent p/n 54855-67604, qty = 2.
- Calibration cable.
- BNC shorting cap.

Figure 104 below shows a drawing of the above connector items.

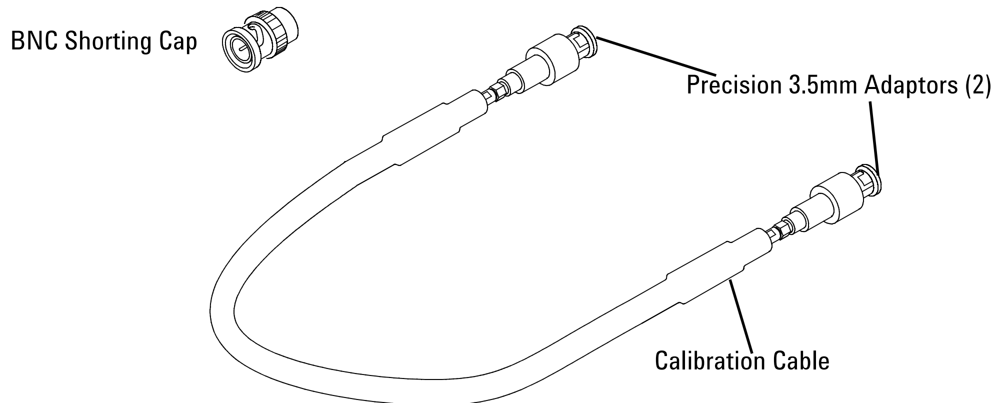


Figure 104 Accessories Provided with the Agilent 54855A Oscilloscope

- 50-ohm Coax Cable with SMA Male Connectors – 24-inch or less RG316/U or similar, qty = 2, matched length.
- SMA T-adapter.
- BNC to SMA male adapter, qty = 1.

Internal Calibration

This will perform an internal diagnostic and calibration cycle for the oscilloscope. For the Agilent oscilloscope, this is referred to as Calibration. This Calibration will take about 20 minutes. Perform the following steps:

1 Set up the oscilloscope with the following steps:
   - a Connect the keyboard, mouse, and power cord to the rear of the oscilloscope.
   - b If SigTest is being used on the oscilloscope, then connect a second monitor to the VGA connector located near the LAN port, on the rear of the oscilloscope.
   - c Plug in the power cord.
   - d Turn on the oscilloscope by pressing the power button located on the lower left of the front panel.
   - e Allow the oscilloscope to warm up at least 30 minutes prior to starting the calibration procedure in step 3 below.

2 Locate and prepare the accessories that will be required for the internal calibration:

   a Locate the BNC shorting cap.

   b Locate the calibration cable.

   c Locate the two Agilent precision SMA/BNC adapters.

   d Attach one SMA adapter to one end of the calibration cable - hand tighten snugly.

   e Attach the other SMA adapter to the other end of the calibration cable - hand tighten snugly.

3 Referring to Figure 105 below, perform the following steps:

   a Click on the Utilities>Calibration menu to open the Calibration window.

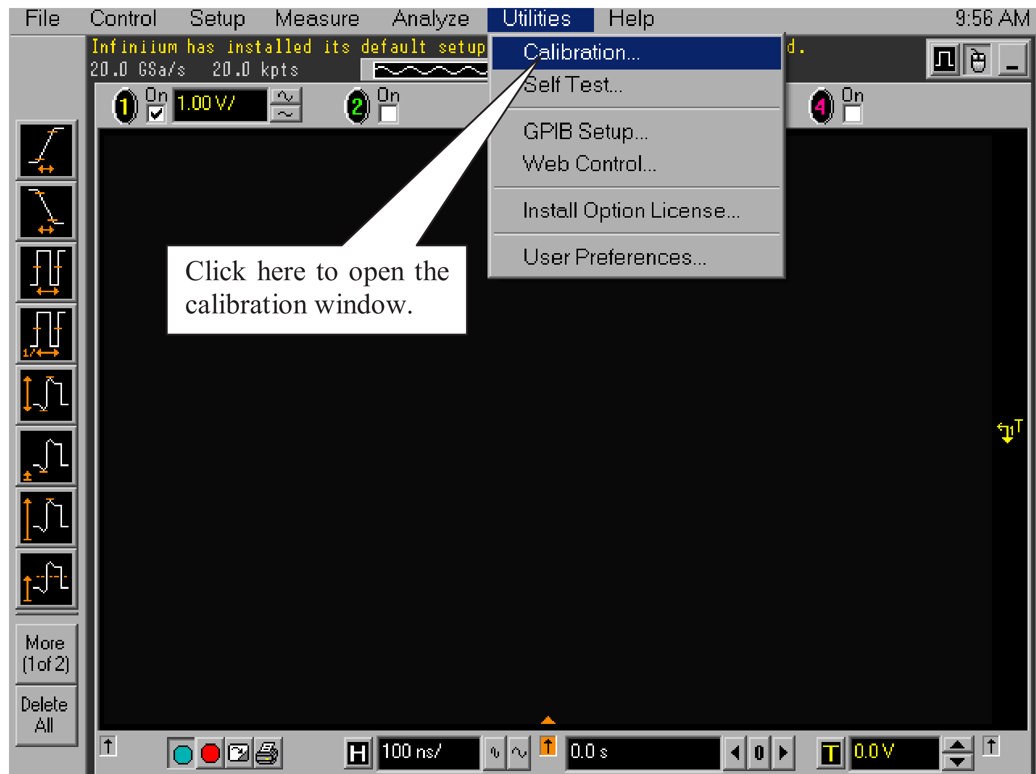


Figure 105 Accessing the Calibration Menu.

4 Referring to Figure 106 below, perform the following steps to start the calibration:

   a Uncheck the Cal Memory Protect checkbox.

   b Click the Start button to begin the calibration.

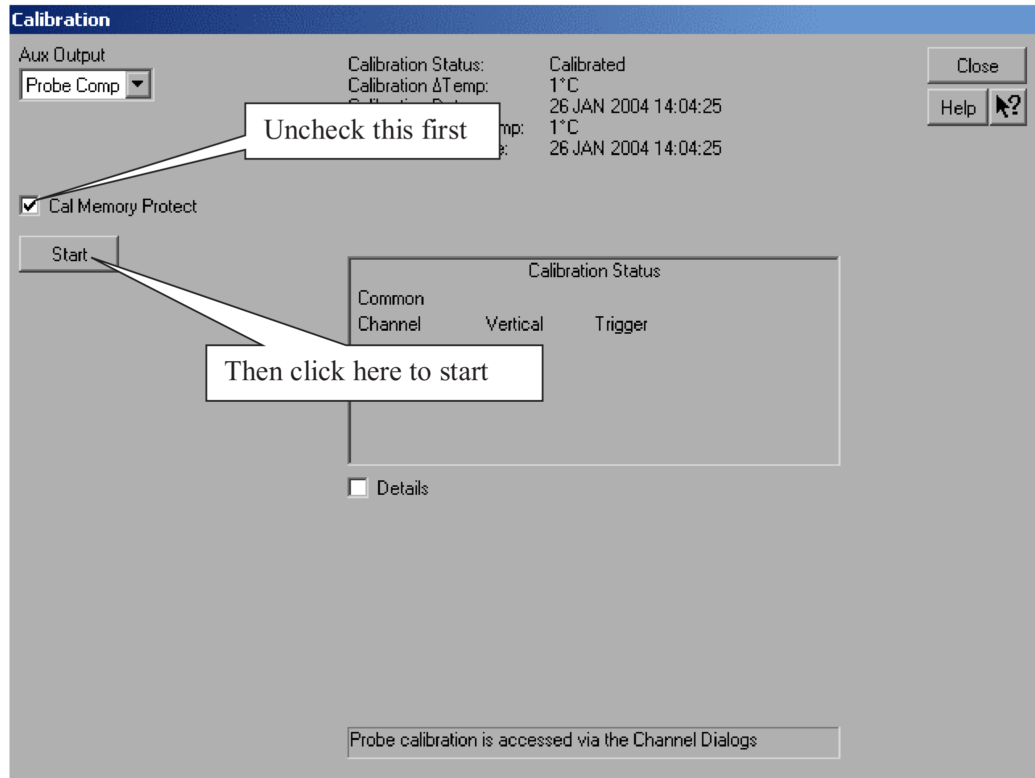


Figure 106 Oscilloscope Calibration Menu.

5 Follow the on-screen instructions:

a You will be prompted to disconnect everything from all the inputs, click the OK button.

b Then, you will be prompted to connect BNC shorting cap to a specified input. Install the BNC shorting cap by pressing it on the specified input BNC, and turning right. Click the OK button after moving the BNC cap to each specified channel.

c Then you will be prompted to connect the calibration cable with SMA adapters between the Aux Out and a specified input, as shown in the example in Figure 107 below. Install the SMA adapter by pressing it on input BNC, and hand tightening the outer ring turning right. Click the OK button after connecting the cable as prompted.

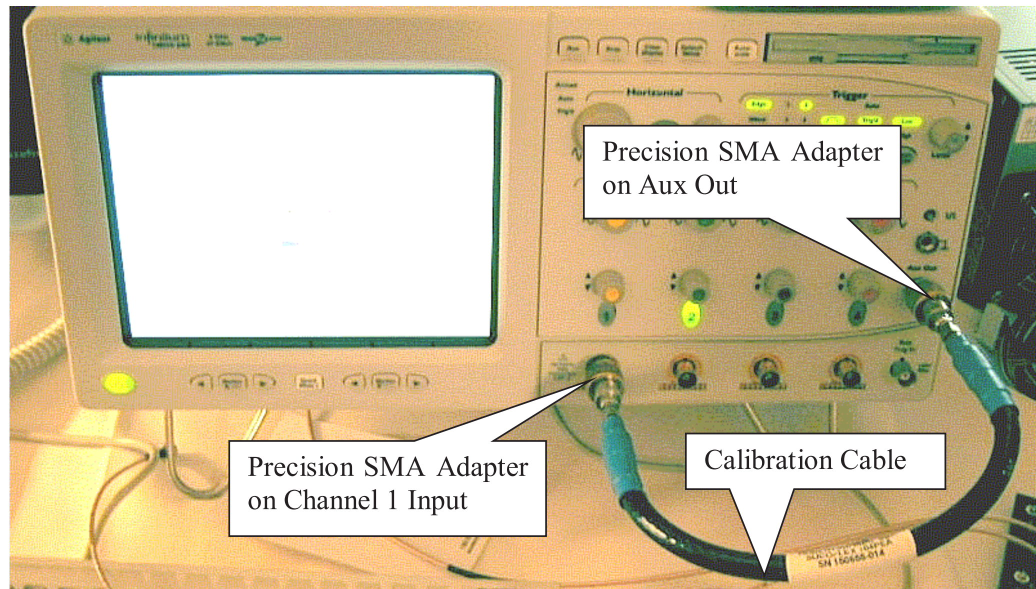


Figure 107 Calibration Cable Connection Example.

- **d** Early during the calibration of channel 1, you will be prompted to perform a Time Scale Calibration, as shown in Figure 108 below.
- **e** Click on the Default button to continue the calibration, using the Factory default calibration factors.
- **f** When the calibration procedure is complete, you will be prompted with a Calibration Complete message window. Click the OK button to close this window.

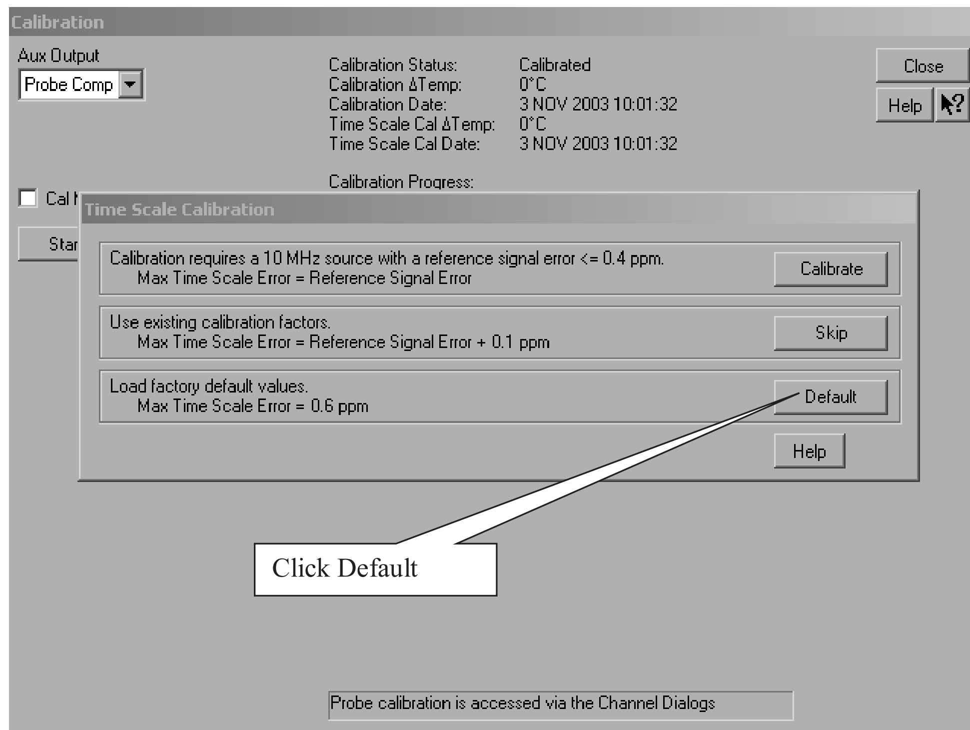


Figure 108 Time Scale Calibration Menu.

6 Referring to Figure 109 below, perform the following steps:

a Confirm that the Vertical and Trigger Calibration Status for all Channels passed.

b Click the Close button to close the calibration window.

c The internal calibration is completed.

d Read NOTE below.

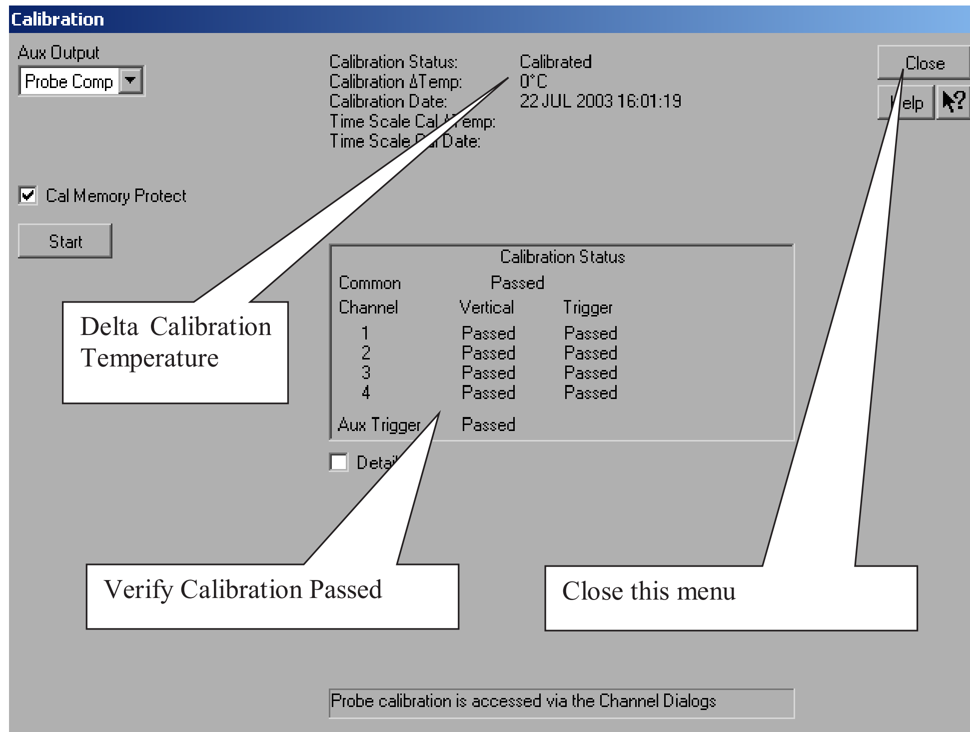


Figure 109 Calibration Status Screen.

NOTE

These steps do not need to be performed every time a test is run. However, if the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, this calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

Cable and Probe Calibration

Perform a 50-ohm direct-coupled input calibration for the SMA interface of channel 1 and channel 3. This calibration compensates for gain, offset, and skew errors in cables and probes. Perform the following steps.

1 Referring to the Figure 110 below, perform the following steps:

   a Locate and connect one of the Agilent precision SMA adapters to the Channel 1 oscilloscope input.

   b Locate and connect the other Agilent precision SMA adapter to the Channel 3 oscilloscope input.

   c Locate and connect one end of one of the RG-316 cables to the SMA adapter on Channel 1.

   d Locate and connect one end of the other RG-316 cable to the SMA adapter on Channel 3.

   e Locate and connect the non-Agilent SMA/BNC adapter to the Aux Out BNC on the oscilloscope.

   f Connect the other end of the cable attached to Channel 1 to the SMA adapter on the Aux Out.

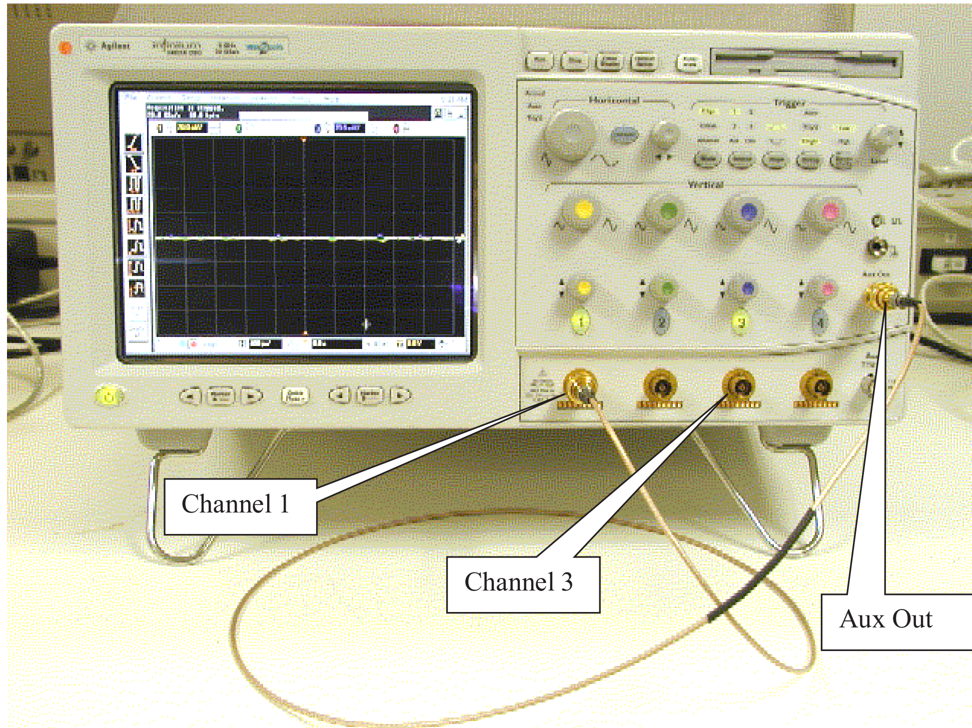


Figure 110 Vertical Input Calibration Connections (Cable on Channel 3 not shown).

2 Referring to Figure 111 below, perform the following steps:

a Click on the Setup>Channel 1 menu to open the Channel Setup window.

b Click the Probes button in the Channel Setup window, to open the Probe Setup window.

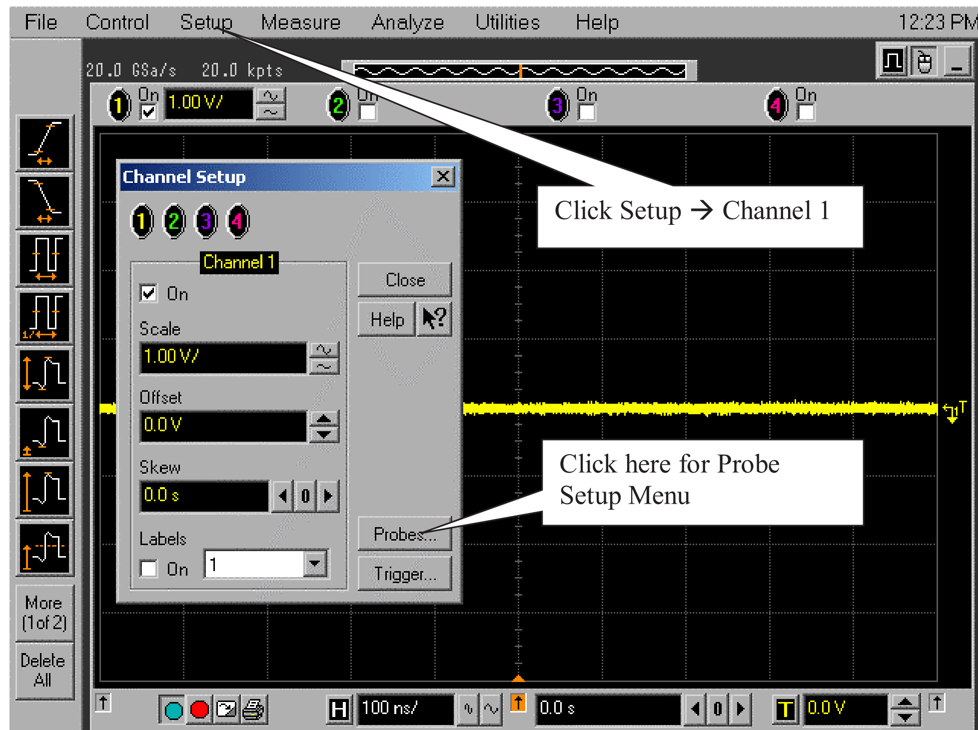


Figure 111 Channel Setup Window.

3 Referring to Figure 112 below, perform the following steps:

a Click the Configure Probing System button, and then click on User Defined Probes.

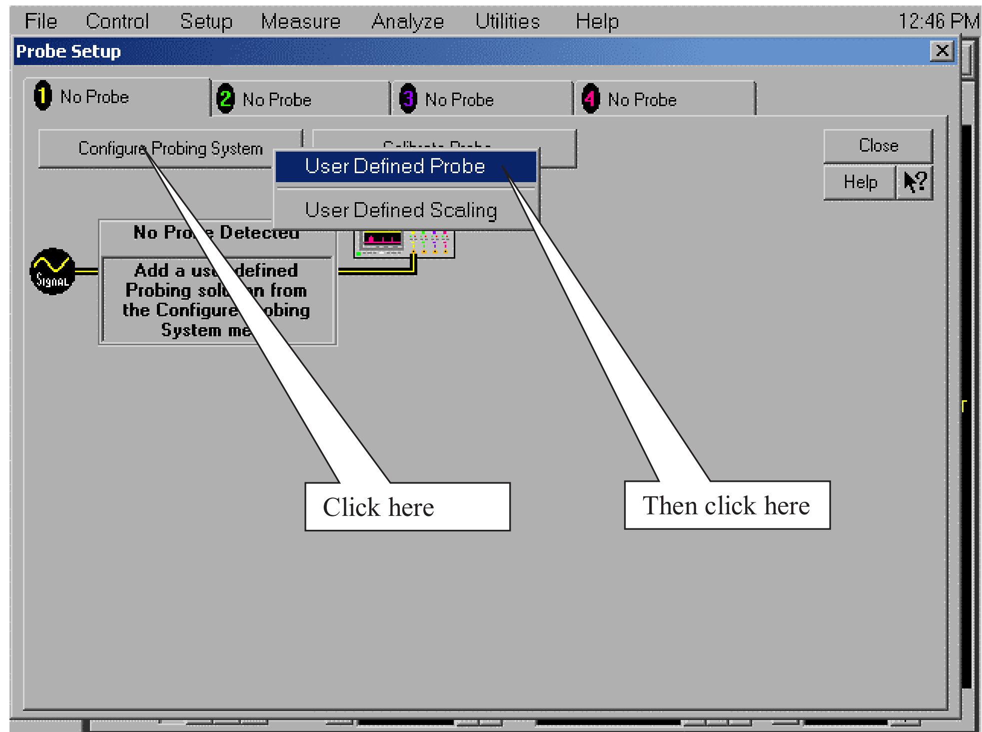


Figure 112 Probe Setup Window.

4 Referring to Figure 113 below, perform the following steps:

a Click on the Calibrate Probe button to open the Probe Calibration window.

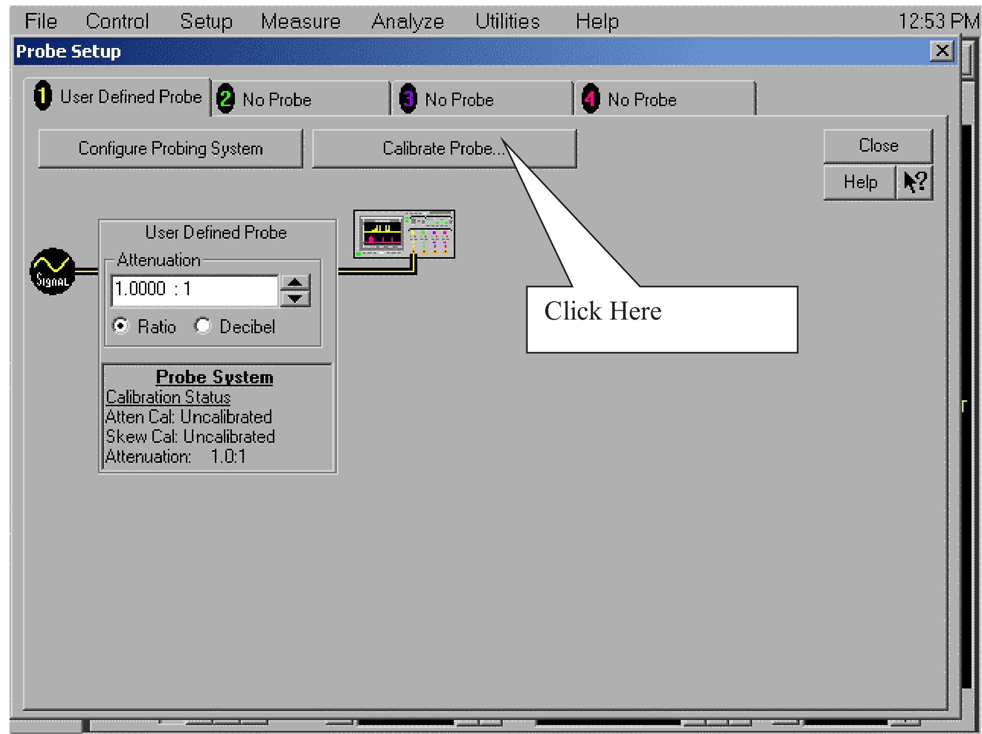


Figure 113 User Defined Probe Window.

5 Referring to Figure 114 below, perform the following steps:

a Select the Calibrated Atten/Offset Radio Button

b Click the Start Atten/Offset Calibration Button to open the Calibration window.

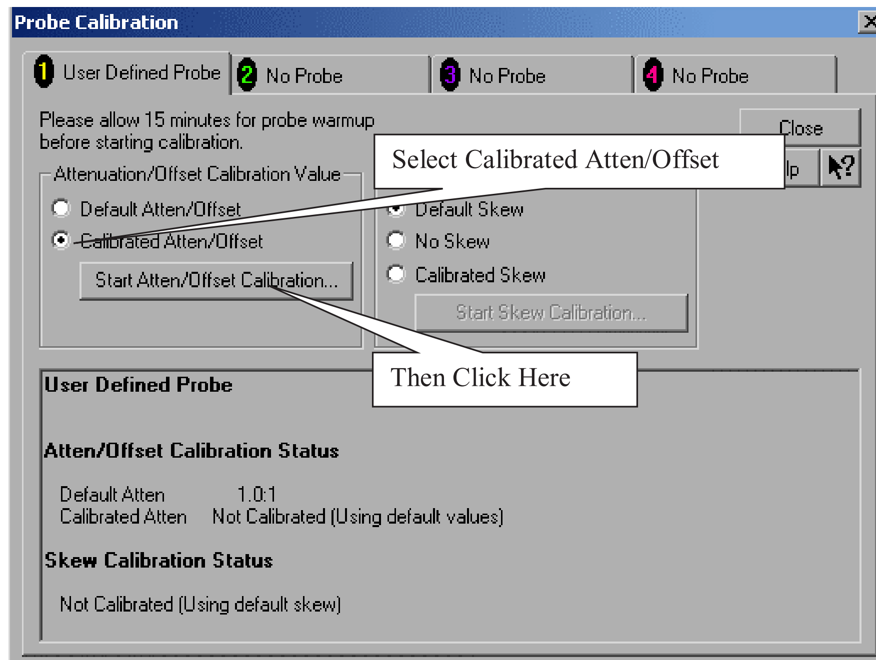


Figure 114 Probe Calibration Window.

6 Referring to Figure 115 shown below, perform the following steps:
   a Ignore the instructions shown in the dialog box.
   b Click the OK button on the Calibration window.
   c The calibration should complete in about 10 seconds.

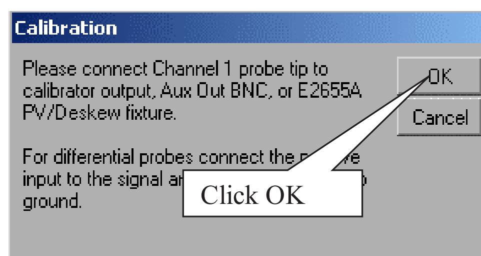


Figure 115 Calibration Window.

7 Referring to Figure 116 below, perform the following steps:
   a Click OK to close the Probe Calibration Done window.

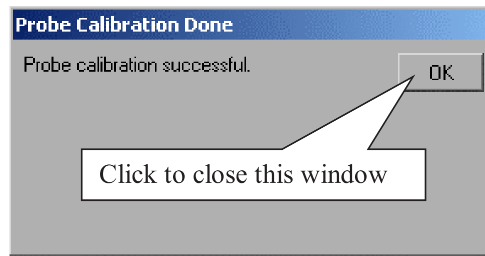


Figure 116 Probe Calibration Done Window.

8 Referring to Figure 117 below, perform the following steps:
   a Select the Calibrated Skew Radio button in the Probe Calibration window
   b Click the Start Skew Calibration button

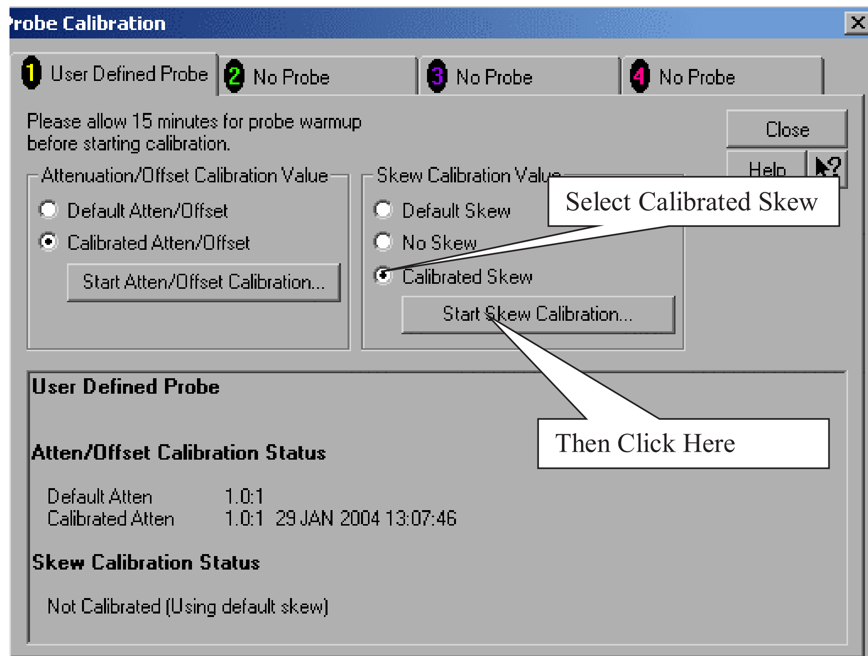


Figure 117 Probe Calibration Window.

9 Referring to Figure 118 shown below, perform the following steps:
   a Ignore the instructions shown in the dialog box.
   b Click the OK button on the Calibration window.
   c The calibration should complete in about 10 seconds.

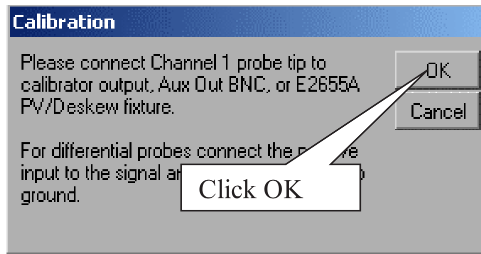


Figure 118 Calibration Window.

10 Referring to Figure 119 below, perform the following steps:

  a Click OK to close the Probe Calibration Done window.

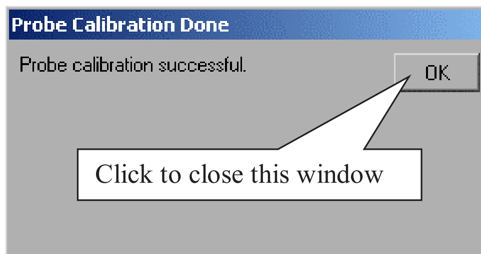


Figure 119 Calibration Window.

11 Referring to Figure 120 below, perform the following steps:

a Click the Close button to close this window.

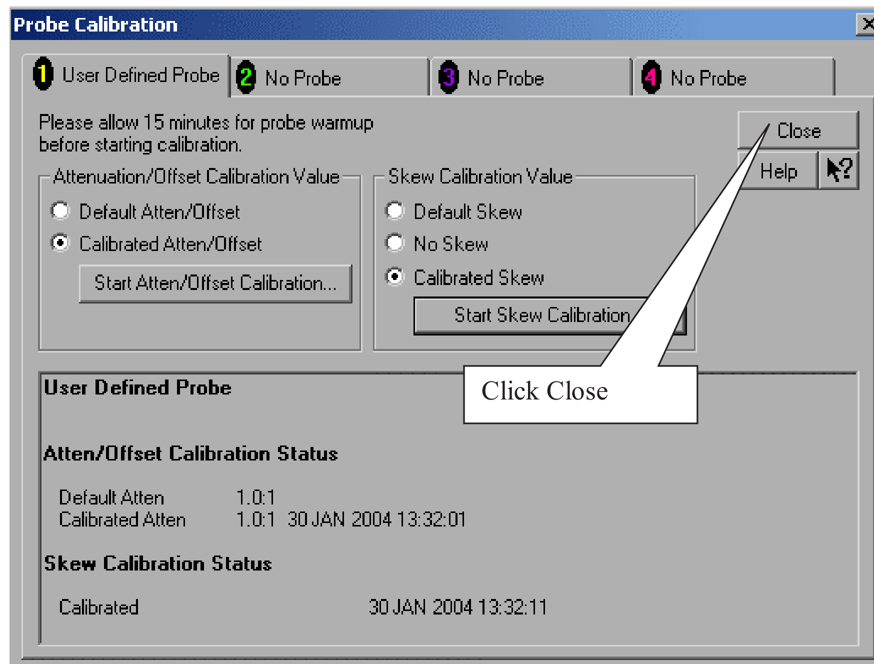


Figure 120 Calibration Window.

12 Referring to Figure 121 below, perform the following steps:

a Click on the Channel 3 tab.

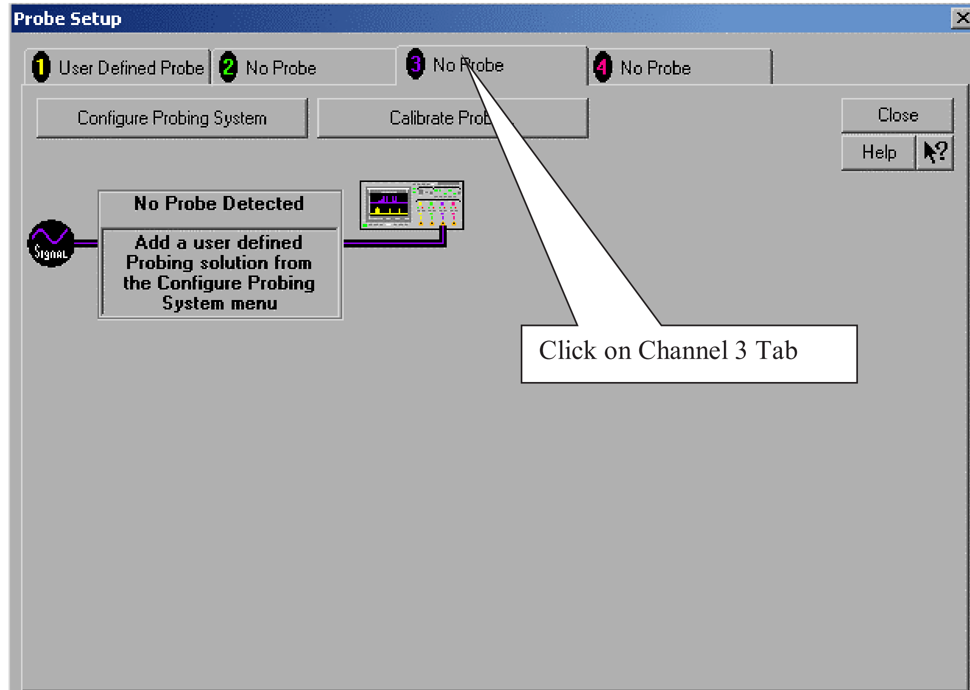


Figure 121 Calibration Window.

13 Referring to Figure 110 on page 377, perform the following steps:

a Disconnect the RG-316 cable connected to the SMA adapter on the Aux Out.

b Connect the other end of the RG-316 cable connected to the SMA adapter on Channel 3, to the SMA adapter on the Aux Out.

14 Repeat steps 3 through 11 of this section to calibrate the cable on Channel 3.

15 Click the Close button on the Probe Setup window (Figure 121) to close this window.

16 Click the Close button on the Channel Setup window (Figure 111 on page 378) to close this window.

17 The Cable and Probe calibration is complete.

18 Read the NOTE below.

NOTE Each cable is now calibrated for the oscilloscope channel it is connected to. Do not switch cables between channels or other oscilloscopes, or it will be necessary to calibrate them again. It is recommended that the cables be labeled with the channel they were calibrated for.

Channel-to-Channel De-skew

This procedure ensures that the timing skew errors between channel 1 and channel 3 are minimized. Perform the following steps:

1 Referring to Figure 122 below, perform the following steps:
   a Do not disconnect the RG-316 cables from either the Channel 1 or Channel 3 SMA adapters.
   b If not already installed, install the non-Agilent SMA adapter on the oscilloscope Aux Out.
   c Disconnect any cable connected to the SMA adapter on the Aux Out.
   d Locate and connect the middle branch of the SMA Tee to the SMA adapter on the Aux Out BNC.
   e Connect the far end of the cable from the Channel 1 SMA adapter, to one branch of the SMA Tee on the Aux Out.
   f Connect the far end of the cable from the Channel 3 SMA adapter, to the other branch of the SMA Tee on the Aux Out.

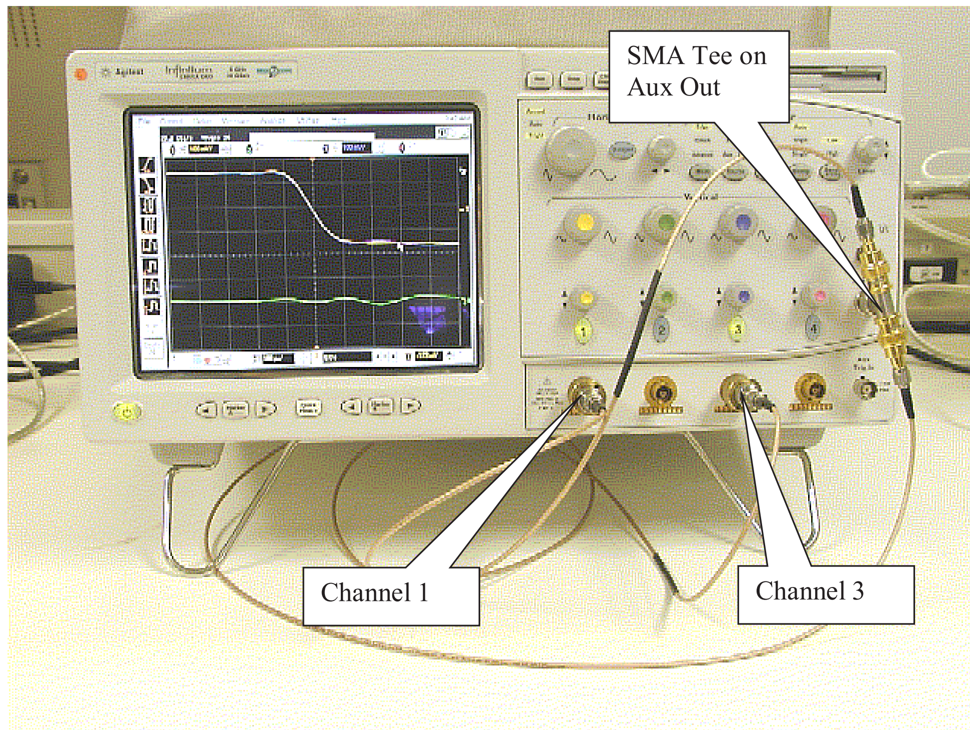


Figure 122 De-skew Connection.

2 Referring to Figure 123 below, perform the following steps:

   a Select the File>Load>Setup menu to open the Load Setup window.

   b Navigate to the directory location that contains the INF_SMA_Deskew.set setup file. If the setup file is not available, it can be created by following the instructions in Appendix C, "INF_SMA_Deskew.set Setup File Details".

   c Select the INF_SMA_Deskew.set setup file by clicking on it.

   d Click the Load button to configure the oscilloscope from this setup file.

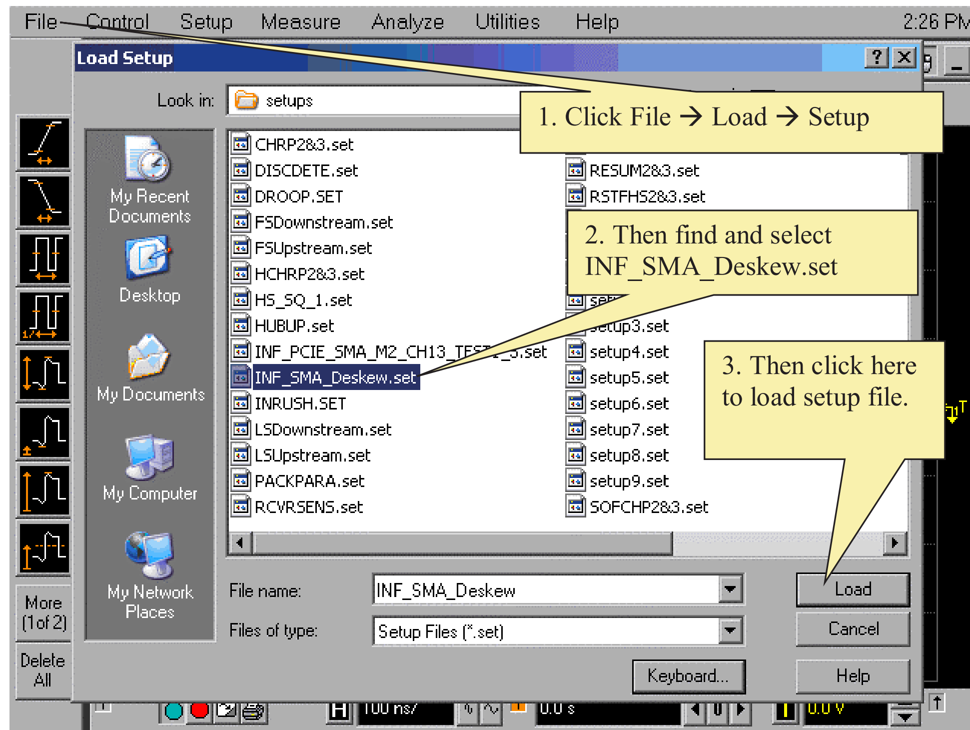


Figure 123 Load De-skew Setup.

The oscilloscope display should look similar to Figure 124 below. A falling edge of the square wave is shown in a 200 ps/div horizontal scale. The upper portion of the screen shows channel 1 (yellow trace) and channel 3 (purple trace) superimposed on one another. The lower portion of the screen is the differential signal (green trace) of channel 1 minus channel 3. The top two traces provide for visual inspection of relative time skew between the two channels. The bottom trace provides for visual presentation of unwanted differential mode signal resulted from relative channel skew (and to a much lesser extent from other inevitable channel mismatch parameters like gain and non-linearity). Figure 124 is an example of exaggerated skew between channel 1 and channel 3, measured to be about 50 ps with the cursor.

Figure 124 Channel Skew.

Figure 125 below shows the desired effect of no skew between the cables. Note that the channel 1 (yellow trace), channel 3 (purple trace) traces overlap, and the differential signal (green trace) is flat. If this is not the case, then perform the following steps to reduce the skew between channels 1 and 3.

Figure 125 Skew Minimized.

3 Referring to Figure 126, perform the following steps to de-skew the channels:

a Click on the Setup>Channel 1 menu to open the Channel Setup window.

b Move the Channel Setup window to the left so you can see the traces.

c Adjust the Skew by clicking on the < or > arrows, to achieve the flattest response on the differential signal (green trace).

d Click the Close button on the Channel Setup window to close it.

e The de-skew operation is complete.

f Disconnect the cables from the Tee on the Aux Out BNC. Leave the cables connected to the Channel 1 and Channel 3 inputs.

g Read the NOTE below.

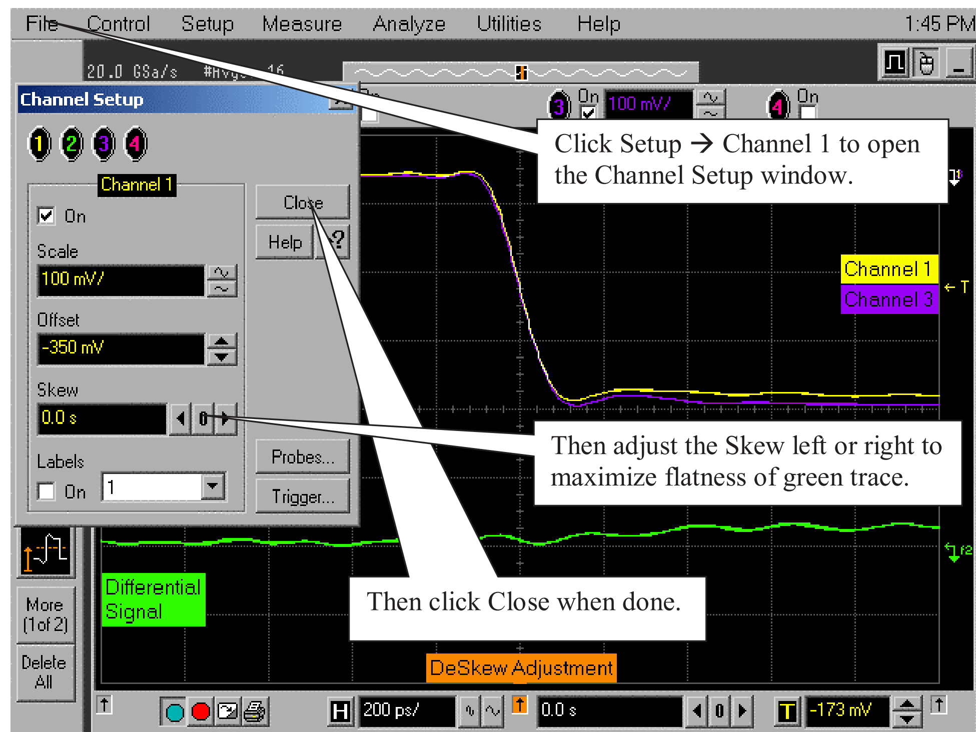
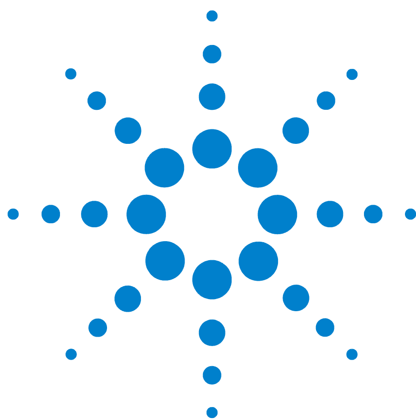


Figure 126 De-skewing Procedure.

NOTE

Each cable is now calibrated for the oscilloscope channel it is connected to. Do not switch cables between channels or other oscilloscopes, or it will be necessary to calibrate them again. It is recommended that the cables be labeled with the channel they were calibrated for.



B
InfiniiMax Probing Options

Figure 127 1134A InfiniiMax Probe Amplifier

Figure 128 1134A Probe Amplifier and E2675A Differential Browser Probe Head

Agilent recommends 1169A or 1134A probe amplifiers. PCI Express 2.0 requires minimum of 1169A probe amplifiers. Agilent also recommends either the E2677A differential solder-in probe head or the E2675A differential browser probe head.

The differential solder-in probe head (E2677A) is recommended for highest signal fidelity while the differential browser probe head (E2675A) may be used for probing convenience.

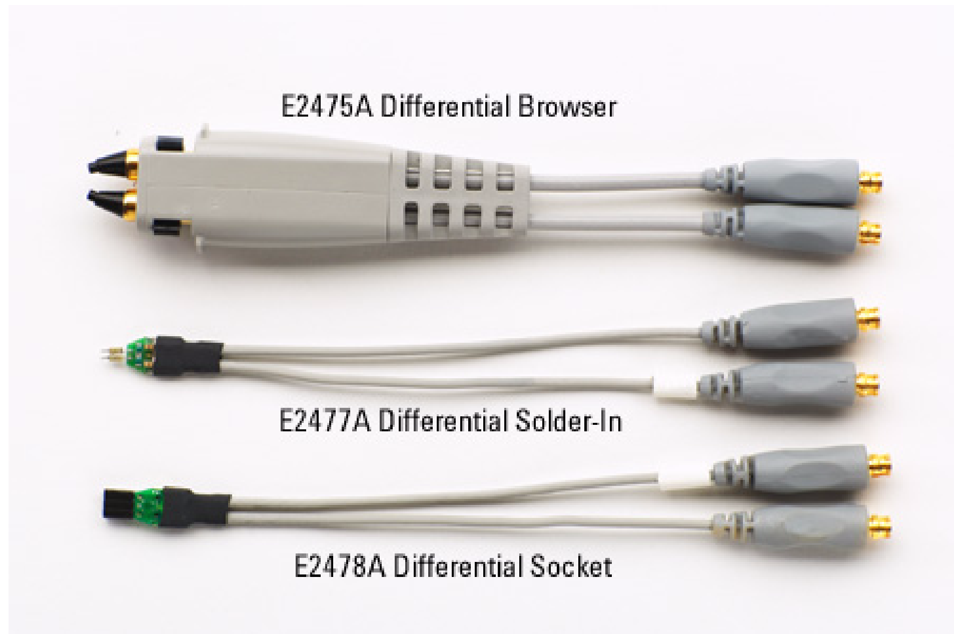
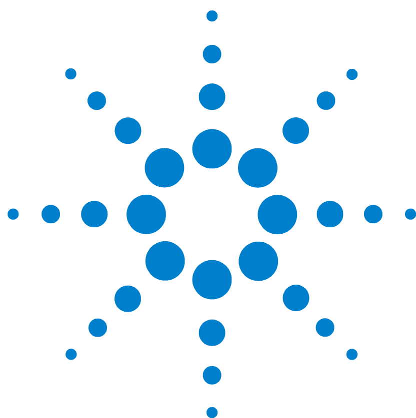


Figure 129 Recommended Probe Heads for the PCI Express Testing

Table 211 Probe Head Characteristics

Probe Head	Model Number	Differential Measurement (BW, input C, input R)	Single-Ended Measurement (BW, input C, input R)
Differential browser	E2675A	6 GHz, 0.32 pF, 50 kOhm	6 GHz, 0.57 pF, 25 kOhm
Differential solder-in	E2677A	7 GHz, 0.27 pF, 50 kOhm	7 GHz, 0.44 pF, 25 kOhm
Differential socket	E2678A	7 GHz, 0.34 pF, 50 kOhm	7 GHz, 0.56 pF, 25 kOhm



C
INF_SMA_Deskew.set Setup File Details

If the INF_SMA_Deskew.set file is not available, you can create it by following these instructions.

1 Start from a default setup by pressing the Default Setup key on the front panel. Then configure the following settings:

Acquisition	Averaging on number of averages 16 Interpolation on
Channel 1	Scale 100.0 mV/ Offset –350mV Coupling DC Impedance 50 Ohms
Channel 3	Turn Channel On; Scale 100.0 mV/ Offset –350m V Coupling DC Impedance 50 Ohms
Time base	Scale 200 ps/sec
Trigger	Trigger level –173mV Slope falling
Function 2	Turn on and configure for channel 1 subtract channel 3, Vertical scale 50 mV/ Offset 100.000 mV

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